

Programmable Keyboard/Display Interface - 8279

A programmable keyboard and display interfacing chip.

Scans and encodes up to a 64-key keyboard.

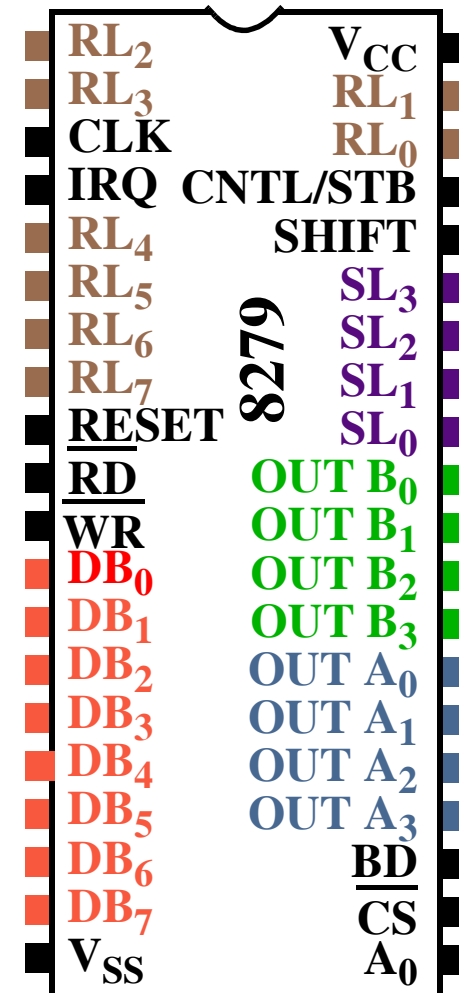
Controls up to a 16-digit numerical display.

Keyboard section has a built-in FIFO 8 character buffer.

The display is controlled from an internal 16x8 RAM that stores the coded display information.

Pinout Definition 8279

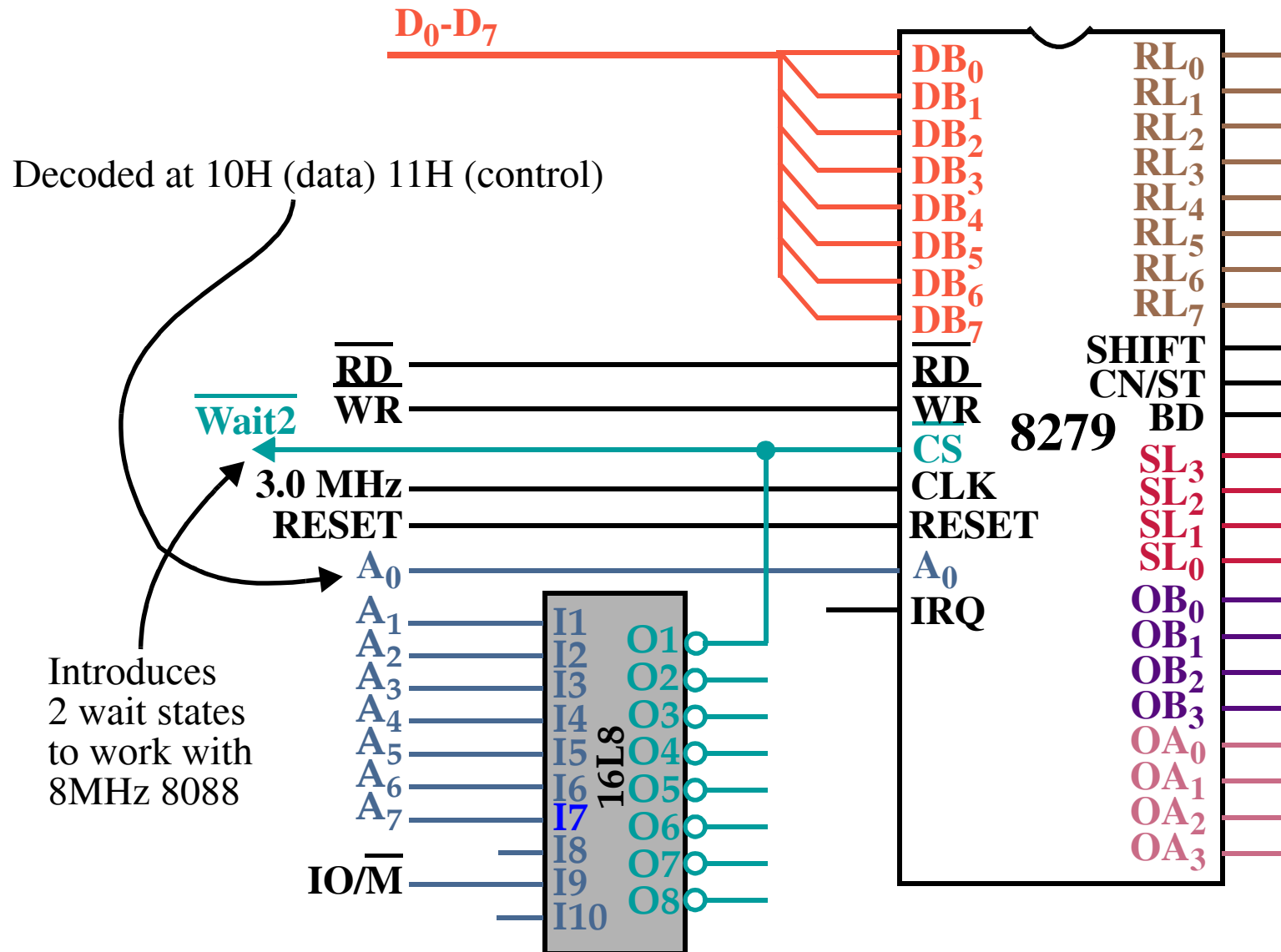
- A0: Selects data (0) or control/status (1) for reads and writes between micro and 8279.
- $\overline{\text{BD}}$: Output that blanks the displays.
- CLK: Used internally for timing. Max is 3 MHz.
- CN/ST: Control/strobe, connected to the control key on the keyboard.



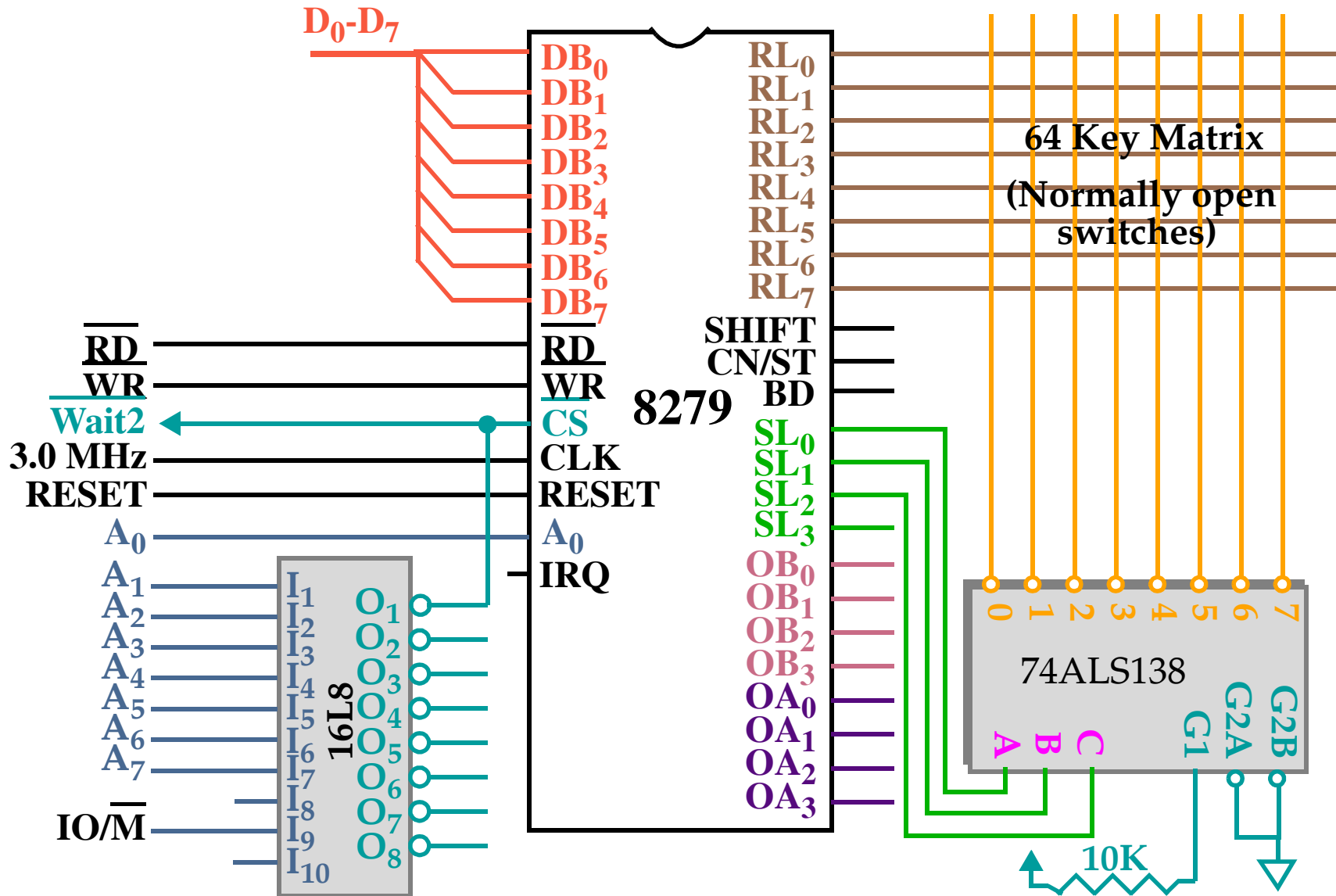
Pinout Definition 8279

- $\overline{\text{CS}}$: Chip select that enables programming, reading the keyboard, etc.
- $\text{DB}_7\text{-DB}_0$: Consists of bidirectional pins that connect to data bus on micro.
- IRQ : Interrupt request, becomes 1 when a key is pressed, data is available.
- $\text{OUT A}_3\text{-A}_0/\text{B}_3\text{-B}_0$: Outputs that sends data to the most significant/least significant nibble of display.
- $\overline{\text{RD}}(\overline{\text{WR}})$: Connects to micro's $\overline{\text{IORC}}$ or $\overline{\text{RD}}$ signal, reads data/status registers.
- RESET : Connects to system RESET.
- $\text{RL}_7\text{-RL}_0$: Return lines are inputs used to sense key depression in the keyboard matrix.
- Shift : Shift connects to Shift key on keyboard.
- $\text{SL}_3\text{-SL}_0$: Scan line outputs scan both the keyboard and displays.

8279 Interfaced to the 8088



Keyboard Interface of 8279



Keyboard Interface of 8279

The keyboard matrix can be any size from 2x2 to 8x8.

Pins SL_2 - SL_0 sequentially scan each column through a counting operation.

The 74LS138 drives 0's on one line at a time.

The 8279 scans RL pins synchronously with the scan.

RL pins incorporate internal pull-ups, no need for external resistor pull-ups.

The 8279 must be programmed first.

D_7	D_6	D_5	<i>Function</i>	<i>Purpose</i>
0	0	0	Mode set	Selects the number of display positions, type of key scan...
0	0	1	Clock	Programs internal clk, sets scan and debounce times.
0	1	0	Read FIFO	Selects type of FIFO read and address of the read.
0	1	1	Read Display	Selects type of display read and address of the read.
1	0	0	Write Display	Selects type of write and the address of the write.
1	0	1	Display write inhibit	Allows half-bytes to be blanked.
1	1	0	Clear	Clears the display or FIFO
1	1	1	End interrupt	Clears the IRQ signal to the microprocessor.

The first 3 bits of the byte sent to control port selects one of 8 control words.

Keyboard Interface of 8279

First three bits given below select one of 8 control registers (opcode).

○ *000DDMMM*

Mode set: Opcode 000.

DD sets displays mode.

MMM sets keyboard mode.

DD field selects either:

- 8- or 16-digit display
- Whether new data are entered to the rightmost or leftmost display position.

<i>DD</i>	<i>Function</i>
00	8-digit display with left entry
01	16-digit display with left entry
10	8-digit display with right entry
11	16-digit display with right entry

Keyboard Interface of 8279**MMM field:**

<i>DD</i>	<i>Function</i>
000	Encoded keyboard with 2-key lockout
001	Decoded keyboard with 2-key lockout
010	Encoded keyboard with N-key rollover
011	Decoded keyboard with N-key rollover
100	Encoded sensor matrix
101	Decoded sensor matrix
110	Strobed keyboard, encoded display scan
111	Strobed keyboard, decoded display scan

Encoded: SL outputs are active-high, follow binary bit pattern 0-7 or 0-15.

Decoded: SL outputs are active-low (only one low at any time).

Pattern output: 1110, 1101, 1011, 0111.

Strobed: An active high pulse on the CN/ST input pin strobes data from the RL pins into an internal FIFO for reading by micro later.

2-key lockout/N-key rollover: Prevents 2 keys from being recognized if pressed simultaneously/Accepts all keys pressed from 1st to last.

Interface of 8279

○ *001PPPPP*

The *clock command word* programs the internal clock driver.

The code PPPPP divides the clock input pin (CLK) to achieve the desired operating frequency, e.g. 100KHz requires 01010 for a 1 MHz CLK input.

○ *010Z0AAA*

The *read FIFO control word* selects the address (AAA) of a keystroke from the FIFO buffer (000 to 111).

Z selects auto-increment for the address.

○ *011ZAAAA*

The *display read control word* selects the read address of one of the display RAM positions for reading through the data port.

○ *100ZAAAA*

Selects *write address* -- Z selects auto-increment so subsequent writes go to subsequent display positions.

Interface of 8279

○ *1010WWBB*

The *display write inhibit control word* inhibits writing to either the leftmost 4 bits of the display (left W) or rightmost 4 bits.

BB works similarly except that they blank (turn off) half of the output pins.

○ *1100CCFA*

The *clear control word* clears the display, FIFO or both

Bit F clears FIFO and the display RAM status, and sets address pointer to 000.

If CC are 00 or 01, all display RAM locations become 00000000.

If CC is 10, --> 00100000, if CC is 11, --> 11111111.

○ *1110E000*

End of Interrupt control word is issued to clear IRQ pin in sensor matrix mode

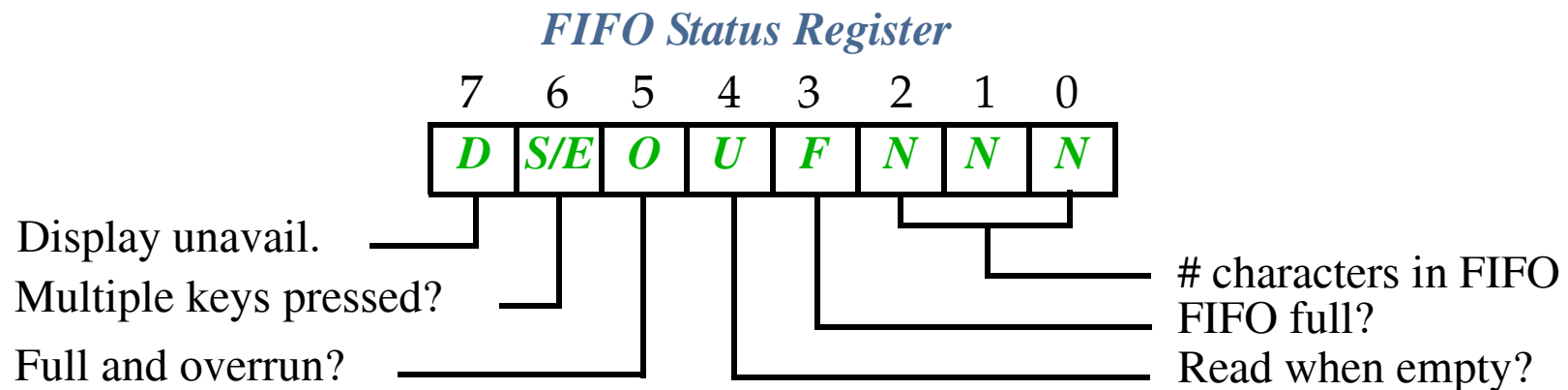
Interface of 8279

- Clock must be programmed first. If 3.0 MHz drives CLK input, PPPPP is programmed to 30 or 11110.
- Keyboard type is programmed next.
 - The previous example illustrates an encoded keyboard, external decoder used to drive matrix.
- Program the FIFO.

Once done, a procedure is needed to read data from the keyboard.

To determine if a character has been typed, the FIFO status register is checked.

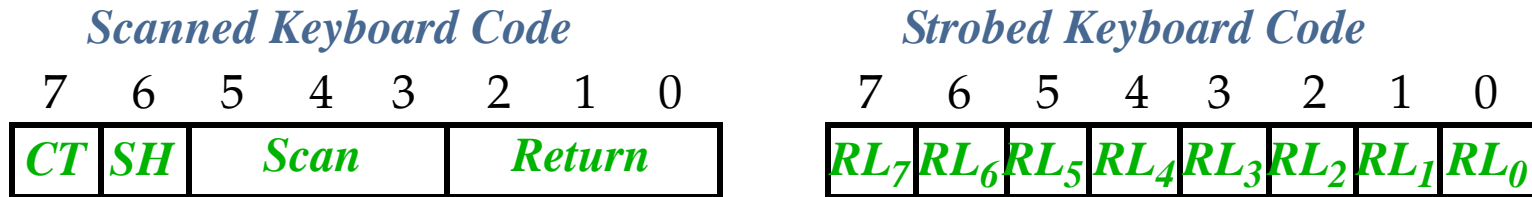
When the control port is addressed by the IN instruction, the contents of the FIFO status word is copied into register AL:



Interface of 8279

Code given in text for reading keyboard.

Data returned from 8279 contains raw data that need to be translated to ASCII:



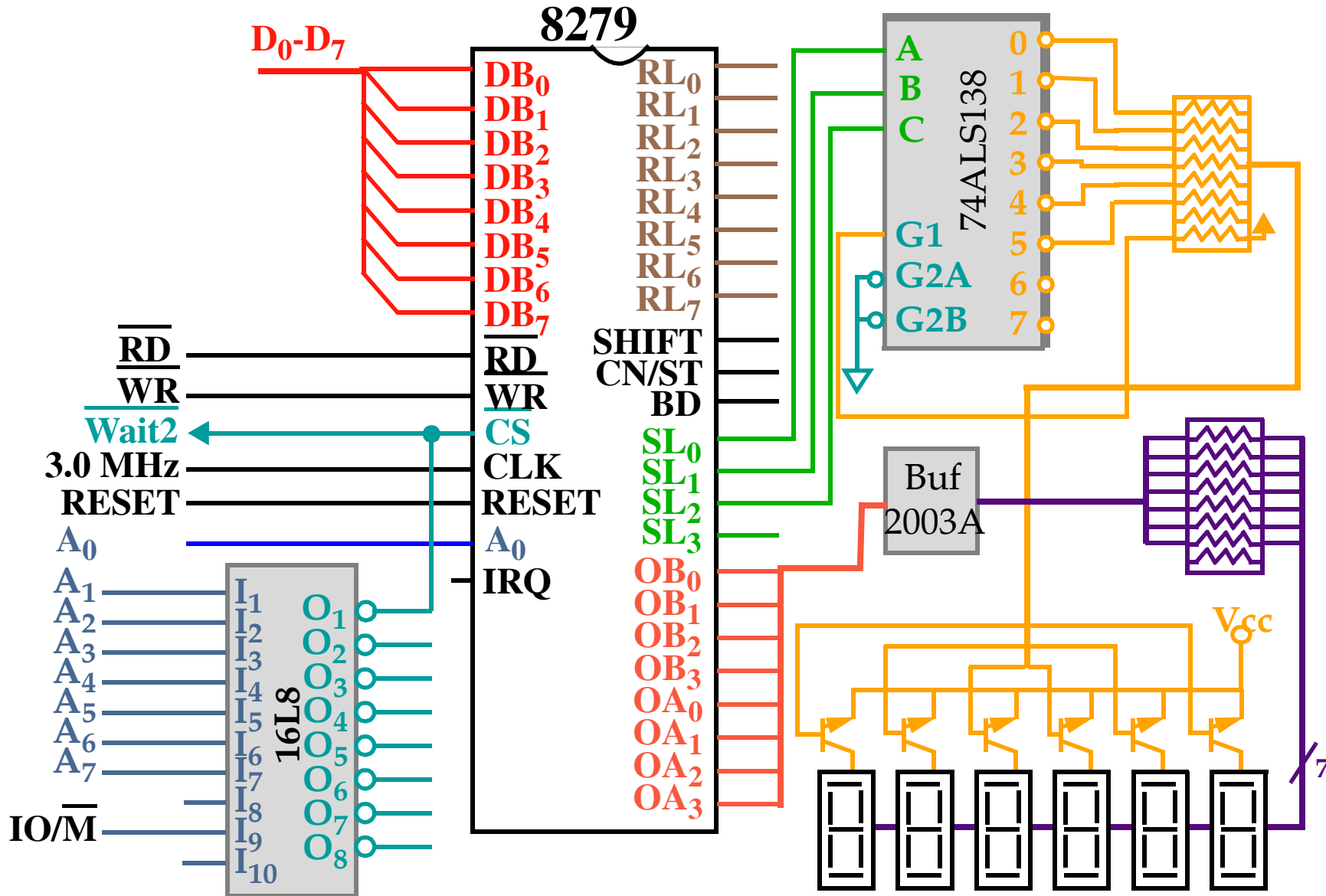
Row and column number are given the rightmost 6 bits (scan/return).

This can be converted to ASCII using the XLAT instruction with an ASCII code lookup table.

The CT and SH indicate whether the control or shift keys were pressed.

The Strobed Keyboard code is just the state of the RL_x bits at the time a 1 was 'strobed' on the strobe input pin.

Six Digit Display Interface of 8279



Programmable Interval Timer: 8254

Three independent 16-bit programmable counters (**timers**).

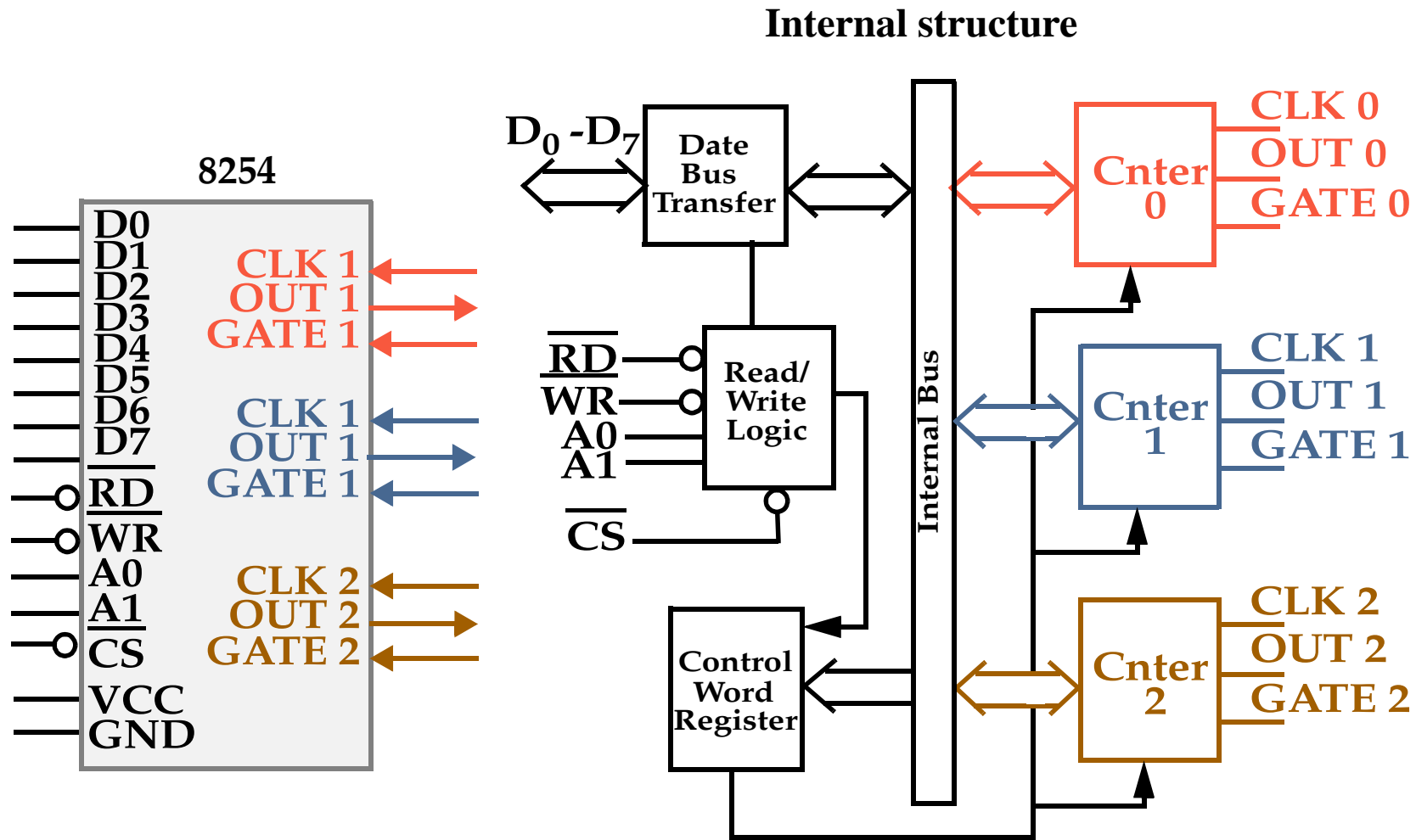
Each capable in of counting in binary or BCD with a maximum frequency of 10MHz.

Used for controlling real-time events such as real-time clock, events counter, and motor speed and direction control.

Usually decoded at port address 40H-43H and has following functions:

- Generates a basic timer interrupt that occurs at approximately 18.2Hz.
Interrupts the micro at interrupt vector 8 for a clock tick.
- Causes DRAM memory system to be refreshed.
Programmed with 15us on the PC/XT.
- Provides a timing source to the internal speaker and other devices.

8254 Functional Description



8254 Pin Definitions

A_1, A_0 : The *address inputs* select one of the four internal registers with the 8254 as follows:

A_1	A_0	Function
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word

CLK : The *clock* input is the timing source for each of the internal counters.

It is often connected to the PCLK signal from the bus controller.

\overline{CS} : *Chip Select* enables the 8254 for programming, and reading and writing.

G : The *gate* input controls the operation of the counter in some modes.

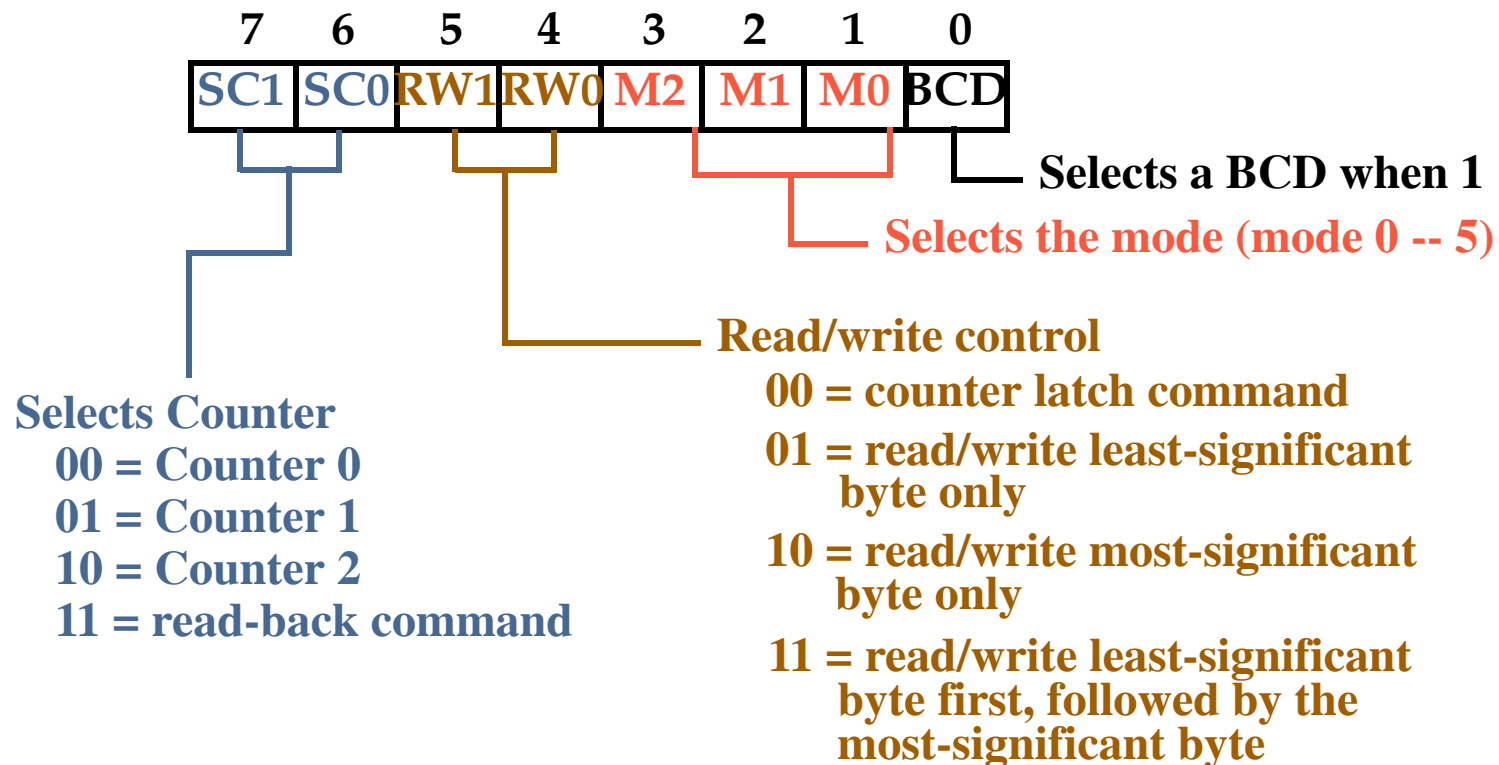
OUT : A *counter output* is where the wave-form generated by the timer is available.

$\overline{RD}/\overline{WR}$: *Read/Write* causes data to be read/written from the 8254 and often connects to the $\overline{IORC}/\overline{IOWC}$.

8254 Programming

Each counter is individually programmed by writing a control word, followed by the initial count.

The control word allows the programmer to select the counter, model of operation, binary or BCD count and type of operation (read/write).



8254 Programming

Each counter may be programmed with a count of 1 to FFFFH.

Minimum count is 1 all modes except 2 and 3 with minimum count of 2.

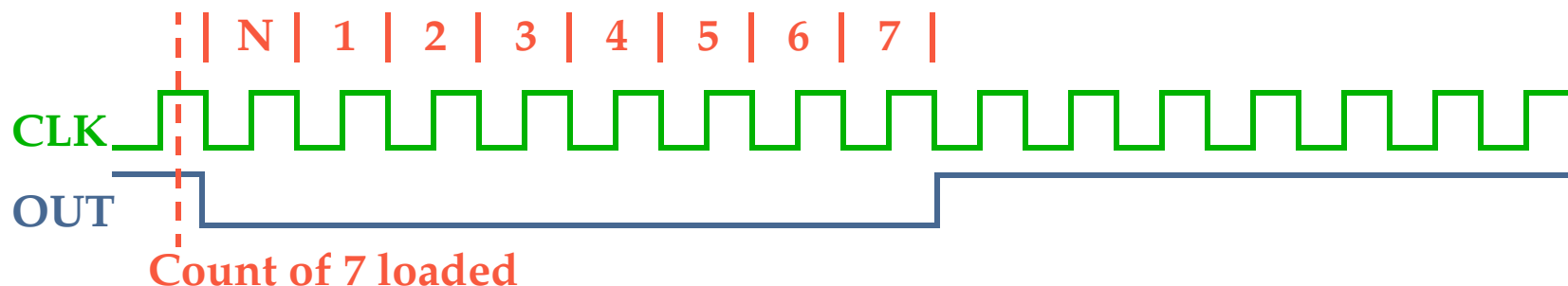
Each counter has a program control word used to select the way the counter operates.

If two bytes are programmed, then the first byte (LSB) stops the count, and the second byte (MSB) starts the counter with the new count.

There are 6 modes of operation for each counter:

○ **Mode 0:** An events counter enabled with G.

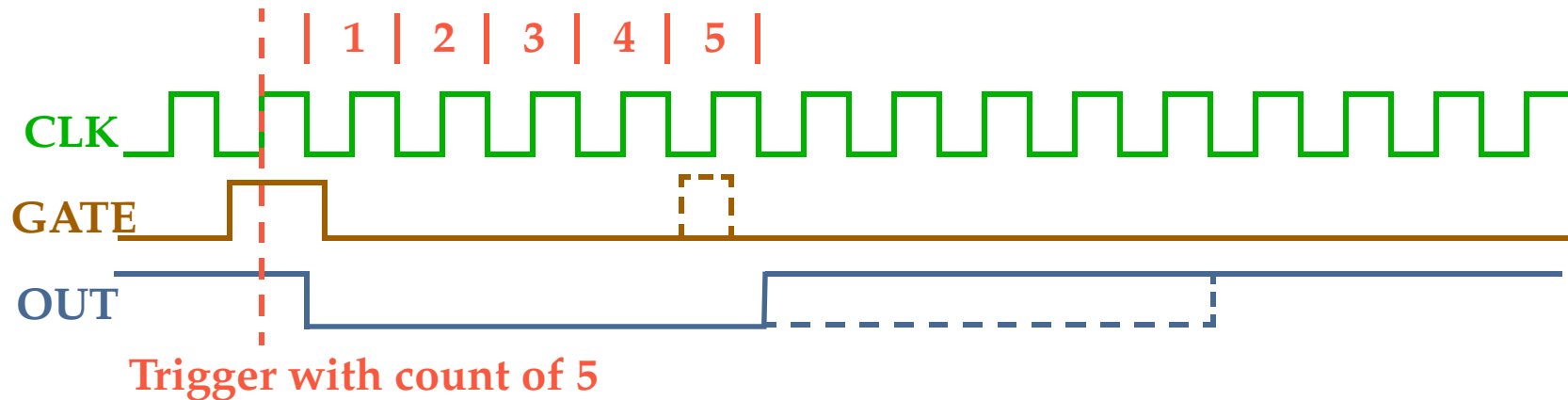
The output becomes a logic 0 when the control word is written and remains there until N plus the number of programmed counts.



8254 Modes

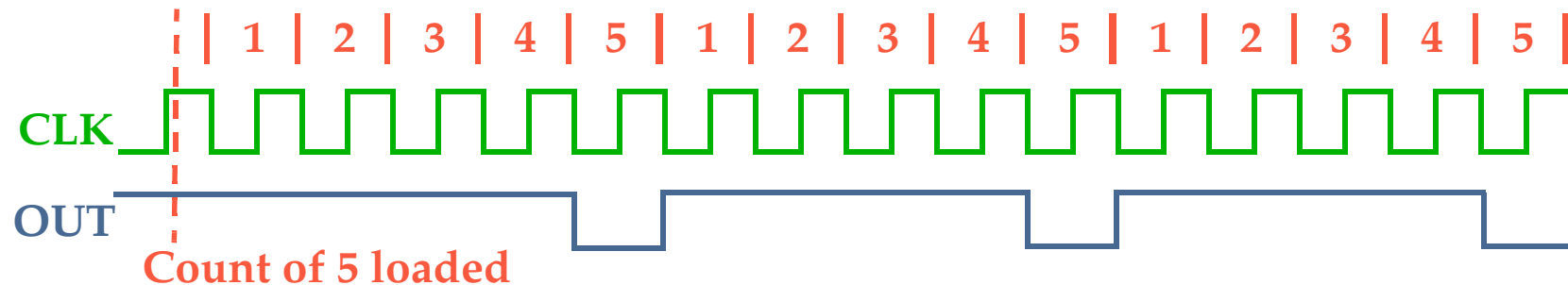
○ Mode 1: One-shot mode.

The G input triggers the counter to output a 0 pulse for $\hat{\text{count}}$ clocks.
Counter reloaded if G is pulsed again.



○ Mode 2: Counter generates a series of pulses 1 clock pulse wide.

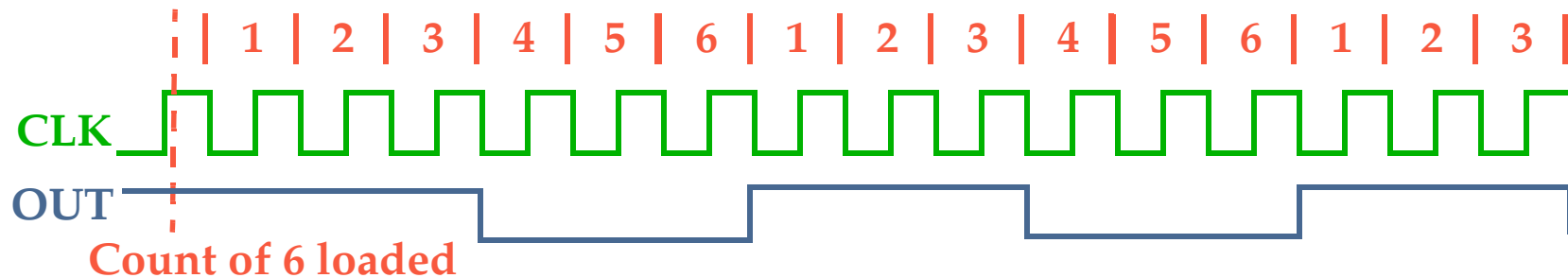
The separation between pulses is determined by the count.
The cycle is repeated until reprogrammed or G pin set to 0.



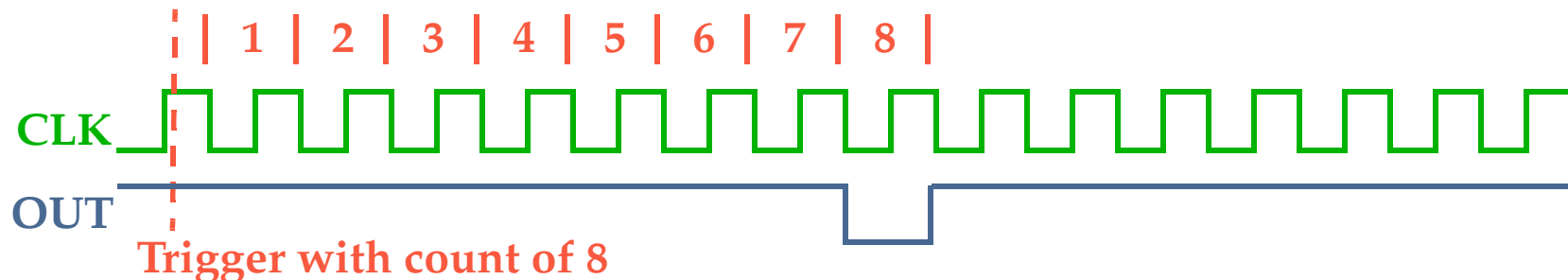
8254 Modes

○ **Mode 3:** Generates a continuous square-wave with G set to 1.

If count is even, 50% duty cycle otherwise OUT is high 1 cycle longer.



○ **Mode 4:** Software triggered one-shot (G must be 1).



○ **Mode 5:** Hardware triggered one-shot. G controls similar to Mode 1.