**Basic I/O Instructions**

**IN** and **OUT** transfer data between an I/O device and the microprocessor's accumulator (AL, AX or EAX).

The I/O address is stored in:
- Register DX as a 16-bit I/O address (variable addressing).
- The byte, p8, immediately following the opcode (fixed address).

**IN** AL, 19H ; 8-bits are saved to AL from I/O port 19H.
**IN** EAX, DX ; 32-bits are saved to EAX.
**OUT** DX, EAX ; 32-bits are written to port DX from EAX.
**OUT** 19H, AX ; 16-bits are written to I/O port 0019H.

Only 16-bits (A₀ to A₁₅) are decoded.
Address connections above A₁₅ are undefined for I/O instructions.

0000H-03XXH are used for the ISA bus.

INS and OUTS transfer to I/O devices using ES:DI and DS:SI, respectively.
**Isolated versus Memory-Mapped I/O**

**Isolated and Memory-Mapped I/O**
- In the Isolated scheme, IN, OUT, INS and OUTS are required.
- In the Memory-mapped scheme, any instruction that references memory can be used.

Disadvantage:
- A portion of the memory space is used for I/O devices.

Advantage:
- IORC and IOWC not required.
- Any data transfer instruction.

Disadvantage:
- Hardware using M/IO and W/R needed to develop signals IORC and IOWC.
- Requires IN, OUT, INS and OUTS.

8-bit port addresses used to access system board device, e.g. timer and keyboard.
16-bit port addresses used to access serial and parallel ports, harddrives, etc.
I/O Map

PCI Bus, user apps and main-board functions

Computer system and ISA Bus

Fixed I/O areas

Variable Port I/O instructions

Fixed Port I/O instructions

I/O Expansion Area

COM 1
Floppy disk
CGI adapter
LPT 1
Hard disk
COM 2
8255(PPI)
Timer
Interrupt controller
DMA controller

0000
0010
0020
0040
0024
0060
0044
0300
0320
0340
02F8
0064
0060
0044
0040
0024
0020
0010
0000
Basic I/O Interface

The basic input device (to the microprocessor) is a set of tri-state buffers. The basic output device (from the microprocessor) is a set of latches.

Basic Input Interface:

8-bit input port

Toggle switches are data source.

When tri-states are enabled, microprocessor can read state of toggle switches into AL (using IN instruction).

I/O port address decoded to SEL
In this case, the data from the OUT instruction is latched using $\overline{SEL}$. D flip-flops hold data from microprocessor. Light-emitting diodes emit when Q output is 0.
Handshaking

I/O devices are typically slower than the microprocessor.

Handshaking is used to synchronize I/O with the microprocessor.

A device indicates that it is ready for a command or data (through some I/O pin or port).

The processor issues a command to the device, and the device indicates it is busy (not ready).

The I/O device finishes its task and indicates a ready condition, and the cycle continues.

There are two basic mechanisms for the processor to service a device.

- **Polling: Processor initiated.** Device indicates it is ready by setting some status bit and the processor periodically checks it.

- **Interrupts: Device initiated.** The act of setting a status bit causes an interrupt, and the processor calls an ISR to service the device.
Interfacing Circuitry

The terminal characteristics of the processor must be matched to those of the I/O devices.

**Input Devices:**

They are either:

- TTL (0.0V-0.8V low and 2.0-5.0V high) or compatible.
- Switch-based; usually either open or connected.

These must be conditioned before they can be used properly.

For example, to make a simple (single-pole, single-throw) toggle switch TTL compatible:

This ensures that the output is held at either 0 or logic 1 at all times (it never floats).

![Circuit Diagram]

The value of R can vary between 1K and 10KΩ.
Interfacing Circuitry

Input Devices:

Mechanical switches physically bounce when they are closed (causing them to momentarily open after being closed).

This can cause a problem if they are used as a clocking signal.

Two asynchronous flip-flop solutions are given below:

Cross-coupled NANDs.

More practical inverter implementation

The basic idea is that these flip-flops store the values even if the D/D nodes both float.
Interfacing Circuitry

Output Devices:

Interfacing an output device requires matching the voltage and current relationships of the devices and processor.

Remember that the standard output levels of TTL compatible devices are 0.0 to 0.4V for logic 0 and 2.4V to 5.0V for logic 1.

The current levels are 0.0 to 2.0mA (logic 0) and 0.0 to -400uA (logic 1).

For example:

Light Emitting Diode

Requires 10mA of current to light.

With a minimum high of 2.4V and a 0.7V BE drop, 1.7V falls across the R₂

\[ R₂ = \frac{1.7\text{V}}{0.1\text{mA}} = \approx 17K \]

Microprocessor  \[ \text{Input} \]

Assume ~2.0V falls across the diode and supply is 5V.

\[ R₁ = \frac{3.0\text{V}}{10\text{mA}} = \approx 300\text{Ω} \]

2N2222 has gain of ~100

Base current should be 0.1mA
**I/O Port Decoding**

For memory-mapped I/O, decoding is identical to memory decoding.

For isolated I/O, IORC and IOWC are developed using M/IO and W/R pins of the microprocessor.

The text gives examples of 8-bit decoding and 16-bit decoding, which is a straightforward application of devices we've used for memory decoding.

The I/O banks on the 8086 through the 80386SX are also set up like the memory.
**I/O Port Decoding**

Similar to memory writes, any 8-bit I/O write request requires separate write strobes (BHE and BLE) but read requests do not.

Note that only an 8-bit I/O port address is decoded.
**I/O Port Decoding**

Output devices can be 16-bit in which case BHE is not needed.

Input devices can be 8-bit or 16-bit.
Note that instead of latches, high impedance buffers (74ALS244) are used in these cases.

32-bit ports are becoming more popular because of PCI bus primarily.
The EISA and VESA local bus are also 32-bit buses.

For the 64-bit data buses of the Pentium, the I/O ports can appear in any of the 8 banks.
However, only 32-bit transfers are supported, as there are no 64-bit transfer instructions.
Programmable Peripheral Interface (82C55)

The 82C55 is a popular interfacing component, that can interface any TTL-compatible I/O device to the microprocessor.

It is used to interface to the keyboard and a parallel printer port in PCs (usually as part of an integrated chipset).

Requires insertion of wait states if used with a microprocessor using higher than an 8 MHz clock.

PPI has 24 pins for I/O that are programmable in groups of 12 pins and has three distinct modes of operation.

In the PC, an 82C55 or its equivalent is decoded at I/O ports 60H-63H.
**Pinout of 82C55 PPI**

**Group A**
Port A (PA7-PA0) and upper half of port C (PC7 - PC4)

**Group B**
Port B (PB7-PB0) and lower half of port C (PC3 - PC0)

**I/O Port Assignments**

<table>
<thead>
<tr>
<th>$A_1$</th>
<th>$A_0$</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Port A</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Port B</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Port C</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Command Register</td>
</tr>
</tbody>
</table>
Interfacing the 82C55 PPI

82C55

Port A
(C0H)

Port B
(C2H)

Port C
(C4H)

Command
Register
(C6H)

74ALS138

D7 -- D0

VCC

GND

I/ORC

I/OWC

A1

A2

RESET

82C55

D0

D1

D2

D3

D4

D5

D6

D7

PA0

PA1

PA2

PA3

PA4

PA5

PA6

PA7

PB0

PB1

PB2

PB3

PB4

PB5

PB6

PB7

PC0

PC1

PC2

PC3

PC4

PC5

PC6

PC7

A0

A1

RESET

CS

RD

WR

74ALS138

A7

A3

A4

A6

A5

A0

G1

G2A

G2B
Programming the 82C55

Command Byte A (Programs ports A, B, C)

<table>
<thead>
<tr>
<th>Group A</th>
<th>Group B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port C (PC7 - PC4)</td>
<td>Port C (PC3 - PC0)</td>
</tr>
<tr>
<td>1 = input</td>
<td>1 = input</td>
</tr>
<tr>
<td>0 output</td>
<td>0 = output</td>
</tr>
<tr>
<td>Port A</td>
<td>Port B</td>
</tr>
<tr>
<td>1 = input</td>
<td>1 = input</td>
</tr>
<tr>
<td>0 = output</td>
<td>0 = output</td>
</tr>
<tr>
<td>Mode</td>
<td>Mode</td>
</tr>
<tr>
<td>00 = mode 0</td>
<td>0 = mode 0</td>
</tr>
<tr>
<td>01 = mode 1</td>
<td>1 = mode 1</td>
</tr>
<tr>
<td>1x = mode2</td>
<td></td>
</tr>
</tbody>
</table>

Command Byte B (Sets or resets any bits in port C)

<table>
<thead>
<tr>
<th>Bit set/reset</th>
<th>Selects a bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 = set</td>
<td>0 = reset</td>
</tr>
</tbody>
</table>
**82C55: Mode 0 Operation**

8-Digit Seven Segment LED Display Interface

- **82C55**
  - D0, A0, A7, B0, A1, B7, C0, C7
  - IORC, IOWC
  - Reset
  - IO/M
  - CS
  - RD, WR

- **16L8**
  - I0, O8
  - I10, O1
  - Vcc, Gnd
82C55: Mode 0 Operation

Mode 0 operation causes the 82C55 to function as a buffered input device or as a latched output device.

In previous example, both ports A and B are programmed as (mode 0) simple latched output ports.

Port A provides the segment data inputs to display and port B provides a means of selecting one display position at a time.
   Different values are displayed in each digit via fast time multiplexing.

The values for the resistors and the type of transistors used are determined using the current requirements (see text for details).

Textbook has the assembly code fragment demonstrating its use.

Examples of connecting LCD displays and stepper motors are also given.
82C55: Mode 0 Operation

4x4 keyboard matrix interface

D7 -- D0

Vcc

82C55

IO/M

Reset

16L8

19
**82C55: Mode 0 Operation**

Flow chart of a keyboard-scanning procedure

1. **KEY**
2. **Scan Keys**
3. **Time Delay for de-bounce**
4. **Scan Keys**
5. **Check Keys**
6. **Calculate key code** → **Return**
7. **If key open**
   - **Check Keys**
   - **Scan Keys**
   - **Time Delay for de-bounce**
   - **Scan Keys**
   - **Wait for Keystroke**
8. **If key closed**
   - **Wait for Release**
82C55: Mode 1 Strobed Input

Port A and/or port B function as latching input devices. External data is stored in the ports until the microprocessor is ready.

Port C used for control or handshaking signals (cannot be used for data).

Signal definitions for Mode 1 Strobed Input

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>STB</td>
<td>The <strong>strobe</strong> input loads data into the port latch on a 0-to-1 transition</td>
</tr>
<tr>
<td>IFB</td>
<td><strong>Input buffer full</strong> is an output indicating that the input latch contain information</td>
</tr>
<tr>
<td>INTR</td>
<td><strong>Interrupt request</strong> is an output that requests an interrupt</td>
</tr>
<tr>
<td>INTE</td>
<td>The <strong>interrupt enable signal</strong> is neither an input nor an output; it is an internal bit programmed via the PC4(port A) or PC2(port B) bits.</td>
</tr>
<tr>
<td>PC7,PC6</td>
<td>The port C pins 7 and 6 are general-purpose I/O pins that are available for any purpose.</td>
</tr>
</tbody>
</table>
82C55: Mode 1 Strobed Input

Mode 1 Port A

- INTE A
- PC4 → STB
- PC5 → IBF
- PC3 → INTR
- PC6+7 → I/O

Mode 1 Port B

- INTE B
- PC2 → STB
- PC1 → IBF
- PC0 → INTR

Timing Diagram

- STB
- IBF
- INTR
- RD

(Buffer full)
(Interrupt request)

Data strobed into port
Data read by microprocessor
82C55: Mode 1 Strobed Output

Similar to Mode 0 output operation, except that handshaking signals are provided using port C.

Signal Definitions for Mode 1 Strobed Output

**OBF**  
**Output buffer full** is an output that goes low when data is latched in either port A or port B. Goes low on **ACK**.

**ACK**  
The **acknowledge** signal causes the **OBF** pin to return to 0. This is a response from an external device.

**INTR**  
**Interrupt request** is an output that requests an interrupt

**INTE**  
The **interrupt enable signal** is neither an input nor an output; it is an internal bit programmed via the PC6(port A) or PC2(port B) bits.

**PC5,PC4**  
The port C pins 5 and 4 are general-purpose I/O pins that are available for any purpose.
**82C55: Mode 1 Strobed Output**

### Mode 1 Port A

- INTE A
- PC6 → ACK
- PC7 → OBF
- PC3 → INTR
- PC4+5 → I/O

### Mode 1 Port B

- INTE B
- PC2 → ACK
- PC1 → OBF
- PC0 → INTR

### Timing Diagram

- WR
- OBF
- (Buffer full)
- INTR
- ACK
- (Interrupt request)
- Port
- Data sent to port
- Data removed from port
### I/O

**82C55: Mode 2 Bi-directional Operation**

Only allowed with port A. Bi-directional bused data used for interfacing two computers, GPIB interface etc.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTR</td>
<td><strong>Interrupt request</strong> is an output that requests an interrupt</td>
</tr>
<tr>
<td>OBF</td>
<td><strong>Output buffer full</strong> is an output indicating that the output buffer contains data for the bi-directional bus</td>
</tr>
<tr>
<td>ACK</td>
<td><strong>Acknowledgement</strong> is an input that enables tri-state buffers which are otherwise in their high-impedance state</td>
</tr>
<tr>
<td>STB</td>
<td>The strobe input loads data into the port A latch</td>
</tr>
<tr>
<td>IFB</td>
<td><strong>Input buffer full</strong> is an output indicating that the input latch contains information for the external bi-directional bus</td>
</tr>
<tr>
<td>INTE</td>
<td><strong>Interrupt enable</strong> are internal bits that enable the INTR pin. Bit PC6(INTE1) and PC4(INTE2)</td>
</tr>
<tr>
<td>PC2, PC1 and PC0</td>
<td>Theses port C pins are general-purpose I/O pins that are available for any purpose.</td>
</tr>
</tbody>
</table>
82C55: Mode 2 Bi-directional Operation

Timing diagram is a combination of the Mode 1 Strobed Input and Mode 1 Strobed Output Timing diagrams.