CMPE212 Lab7 MORE Verilog Coding

Objective

To get more experience with Verilog. To perform multiplexing with different logic operators.

Procedure

Connect to your gl account and make a directory for the lab.
I want a top module that will contain submodules. These are the design constraints:

• There will be four logical operators that will be performed NOT, AND, OR, XOR.
• These logical operator modules will take in two 4bit inputs and one 4bit output. Except for NOT, which takes in one 4bit input and one 4bit output.
• The operators will be performed bitwise. So for the AND gate, I want the i-th output to be the AND of the i-th bit of each input.
• The logical operators will go through a multiplexor.
• The switch for the multiplexor will function as such:
  – NOT - 00
  – AND - 01
  – OR - 10
  – XOR - 11

There are many ways to organize your work. Make each logical operator a module of its own. Make one generic four input multiplexor. These can make your job easier and your troubleshooting easier.

Verification

Make sure you show your top module and your output to Zhen.
These are the cases that I want you to check in your testbench:

1. NOT 0101
2. AND 0011, 0101
3. OR 0011, 0101
4. XOR 0011, 0101

Your output should show the 4bit inputs to the top module, the 2bit switch input to the top module, and the 4bit output of the top module.

You can make a testbench for each separate module to verify that their outputs are correct. But we do want a testbench of your top module.