CMPE212 Lab 4 Function Generator, Oscilloscope, and DeMorgan’s laws

Objective

To check that gates cause a time delay and to try to measure how much of a delay. Use that to estimate the length of time for a critical path. To verify DeMorgan’s laws.

Procedure

Part 1

First, we will check time delays caused by the gates. To do this, try these steps:

1. Connect your OR gates, wires, and switch to the breadboard. (Remember, keep track of the direction the notch is in on your IC)
2. Connect one input of each OR gate to ground.
3. Connect the output of all OR gates to an input of another OR gate.
4. Connect the function generator to the appropriate rails of the breadboard.
5. Connect the oscilloscope to the input of the gates (the function generator signal) and the output of your first OR gate.
6. Change the oscilloscope connection from the first OR gate to the last OR gate.
7. Set your function generator to a square wave with 2.5 amplitude and 1.25 offset. Try a lower frequency to make it easier to set oscilloscope.
8. Change the timescale on your oscilloscope so that you can read your waveform.

Part 2

This is just another hardware exercise. Use NOT, AND, and OR gates with two inputs to verify DeMorgan’s Laws. Your choice of doing a NOT of an OR gate or a NOT of an AND gate, but make sure you also build the logically equivalent circuit for your choice.

Questions

1. For part 1, you can get a delayed version of your input using only AND gates also. How would you have to connect the inputs for the AND gates?
2. For part 1, is there some ambiguity on the time delay of the gates? How could we eliminate that ambiguity?
3. For part 1, what is an estimated delay of one of your gates? Is the total delay just the time delay of one gate multiplied by the number of gates?
4. For part 2, using your choice of NOT/OR or NOT/AND combination, what is its logically equivalent circuit?