Atomic layer deposited Ta$_2$O$_5$ gate insulation for enhancing breakdown voltage of AlN/GaN high electron mobility transistors

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AlN/GaN heterostructures with a 3.5 nm AlN cap have been grown by molecular beam epitaxy followed by a 6 nm thick atomic layer deposited Ta$_2$O$_5$ film. Transistors fabricated with 150 nm length gates showed drain current density of 1.37 A/mm, transconductance of 315 mS/mm, and sustained drain-source biases up to 96 V while in the off-state before destructive breakdown as a result of the Ta$_2$O$_5$ gate insulator. Terman’s method has been modified for the multijunction capacitor and allowed the measurement of interface state density ($\sim 10^{13}$ cm$^{-2}$ eV$^{-1}$). Small-signal frequency performance of 75 and 115 GHz was obtained for $f_t$ and $f_{\text{max}}$, respectively. © 2011 American Institute of Physics. [doi:10.1063/1.3531551]

The recent advent of optimized growth of pseudomorphic AlN/GaN high electron mobility transistors (HEMTs)$^{1,2}$ has enabled the demonstration of very high current density (2.3 A/mm), extrinsic transconductance of 0.5 S/mm,$^3$ and small signal frequency performance in excess of 100 GHz.$^4,5$ Such performance sets the stage for the AlN/GaN HEMT to take a leading position in the high frequency/power amplification realm. However, to date, reports show a limited applied $V_{\text{DS}}$ range and low off-state breakdown voltage (<20 V) for GaN-based transistors.$^6$ In order to take advantage of the outstanding current density capability of these devices for high-power applications the accessible bias voltage range must be increased. HEMTs designed with a thin (<6 nm) AlN barrier require a gate insulator for gate leakage current suppression due to an otherwise prevalent tunneling current. Recent reports have demonstrated the use of atomic layer deposited (ALD) Al$_2$O$_3$ or HfO$_2$ for gate insulators to the AlN/GaN HEMT.$^{2,7}$ Yet the off-state breakdown voltage has remained low due primarily to gate insulator failure leading to premature off-state breakdown. One of the highest breakdown voltage reports to date for an AlN/GaN HEMT stated a maximum $V_{\text{DS}}$ of 45 V and a resulting output power density of 850 mW/mm at 2 GHz with $V_{\text{DS}}$=15 V.$^8$ However, the reported devices showed soft pinched-off characteristics and a low drain current density of only 380 mA/mm.

One common technique used for increasing breakdown voltage in HEMTs is the use of field plates.$^9$ However, metallurgical gate extensions drastically increase parasitic capacitance in the device and thus hamper frequency performance. Significant progress has been made with ALD oxides, including Ta$_2$O$_5$, for Si and GaN-based metal-oxide-semiconductor test structures$^{10,11}$ since they provide a high dielectric constant film and are electronically robust. However, Ta$_2$O$_5$ has yet to be investigated for the purpose of gate insulation in GaN HEMT structures. In an effort to improve the range of applied bias voltage of an insulated-gate AlN/GaN HEMT while simultaneously taking advantage of the structure’s inherent scalability, a 6 nm thick ALD Ta$_2$O$_5$ film was deposited for gate current suppression on an AlN/GaN structure with a 3.5 nm thick AlN cap (Fig. 1). With an effective band gap of ~4.4 eV,$^{11}$ a relative dielectric constant value$^{10}$ as high as 20, and a critical breakdown field of approximately 4 MV/cm, Ta$_2$O$_5$ appears favorable for gate insulation where vertical down-scaling imposes high electric fields conditions.

III-N epitaxial layers were grown by plasma assisted molecular beam epitaxy (MBE) on a 2-in semi-insulating 6H-SiC substrate using procedures similar to those described previously.$^{12,13}$ Three cycles of Ga deposition and desorption like that described by Brandt et al.,$^{13}$ were performed in the growth chamber prior to growth. A 60 nm AlN nucleation layer was grown first, followed by a 1 $\mu$m GaN buffer and a 3.5 nm AlN barrier layer. The AlN barrier thickness was chosen on the basis of work by Cao et al. who showed a minimum in sheet resistance in single heterostructure AlN/GaN for AlN thicknesses between 3–4.5 nm.$^4$ All layers were grown without interrupts or doping and at a substrate temperature of 730 °C.

![FIG. 1. (Color online) Layer structure and conduction band diagram of the Ta$_2$O$_5$/AlN/GaN HEMT structure showing pertinent quantities for Terman analysis (D$_s$ illustrated by green dashes). 1×1 $\mu$m AFM scan in upper right corner.](image)

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Device processing was initiated by an Ohmic-first sequence. Ohmic contacts were formed by a shallow premetalization etch prior to the deposition of a Ti/Al/Ni/Au metal stack and an 800 °C anneal. This process yielded a contact resistance ($R_c$) of 0.7 Ω mm as measured by the transmission line method. A 6 nm ALD Ta$_2$O$_5$ layer was blanket deposited following a 100 nm deep, Cl-based, mesa isolation etch. Ta$_2$O$_5$ films were prepared using an ALD process utilizing pentakis(dimethylamino)tantalum (PDMAT) and water as reagents at 250 °C. The films were deposited in a hot wall flow tube type reactor. A constant flow of ultrahigh purity N$_2$ gas (15 sccm) was used to maintain a flow tube pressurization of 200 mTorr during deposition and a 30 s purge time was used to separate the reagent pulses. Under these conditions linear growth was observed and a growth rate of 2.2 Å per cycle as reagents at 250 °C. The films were deposited in a hot wall flow tube type reactor.

Electron-beam lithographic definition of submicron gates with a T-profile concluded the device processing. Pertinent geometric dimensions of the HEMTs were source-drain separation ($L_{SD}$) of 3 μm, gate width ($W_g$) of 2 × 25 μm, and gate footprint length ($L_g$) of ~150 nm. On-wafer room-temperature Hall measurements were taken after the Ta$_2$O$_5$ deposition and sheet resistance was found to be 356 Ω/□ with a two-dimensional electron density and mobility of $2.2\times10^{13}$ cm$^{-2}$ and 800 cm$^2$/V·s, respectively.

Drain characteristics were shown in Fig. 2 with a maximum current density of 1.37 A/mm at $V_{DS} = -7$ V. Transfer characteristics were taken at $V_{DS} = 8$ V and shown in Fig. 3(a). A maximum extrinsic transconductance ($g_{mn}$) was measured to be 315 mS/mm. Taking into account source contact (0.7 Ω mm) and access (0.21 Ω mm) resistance, this value corresponds to an intrinsic $g_{mn} = 450$ mS/mm. Gate current was found to be the limitation in off-state drain current [Fig. 3(b)]. Low ($10^{-8}$ A/mm) parallel conduction in the buffer layer was measured.

Off-state breakdown voltage is often defined by the criterion that 1 mA/mm drain current density is reached in the subthreshold state. According to this metric, $V_{BD} \approx 30$ V. However, the Ta$_2$O$_5$-insulated devices ultimately sustained drain-source voltages of up to 96 V under off-state gate-source bias ($V_{GS} = -7$ V) before destructively breaking down (Fig. 2) demonstrating an ~5× increase of this particular characteristic over other reports. It is noted that after ~60 V drain voltage sweep in off-state conditions, the device’s low-voltage $I_{DS}$ and $g_m$ degraded by 30–50 %. The pre-BDB degradation is speculated to be the result of a localized breakdown of the AlN barrier at the drain edge of the gate under reverse bias forcing the Ta$_2$O$_5$ to sustain the entire voltage drop. This would still maintain transistor action after AlN breakdown but with degraded transport across the gated region. It is therefore plausible that DBD occurs after AlN breakdown when the local electric field is of sufficient intensity to cause electrical failure of the Ta$_2$O$_5$ film.

Terman’s high-frequency C-V method has been adapted for the stacked oxide/barrier structure in order to investigate the Ta$_2$O$_5$/AlN interface. The C-V functionality of the Ta$_2$O$_5$/AlN/GaN structure may be acquired through Poisson’s equation and is found to yield the total “ideal” capacitance: $C_{tot} = (1/C_{ox} + 1/C_{AlN} + 1/C_{Q})^{-1}$. $C_{ox}$ and $C_{AlN}$ are the fixed oxide and AlN barrier capacitances and $C_{Q} = Q_{nit}/kT(1 + e^{-\theta C})^{-1}$ is the quantum capacitance of the GaN well (QW) assuming population of only one subband, $E_c$. $Q_{nit} = m^*kT / \pi \hbar^2$ is the effective conduction band density of states and $\eta_c = (E_F - E_c) / kT$ is the normalized local potential at the GaN QW (see Fig. 1). The assumption of single subband population may lead to some error for conditions that cause high 2DEG population. The Fermi level in the channel is affected by the occupation of interface states which causes C-V stretch-out. The charge-field relationship between the two charge distributions may be found by considering a voltage loop starting from the oxide/AlN interface and terminating at the Fermi level in the GaN QW

$$kT \eta_c - qV_{AIN} - \Delta E_C + E_s + kT \eta_c = 0,$$  

where $kT \eta_c = E_{Ci} - E_F$ is the local potential at the oxide/AlN interface, $V_{AIN} = q \left[ \frac{1}{C_{ox}} - \tau_{ox} \right] / C_{AIN}$ is the voltage drop in the AlN barrier, and $\Delta E_C$ is the AlN/GaN conduction band discontinuity. Interface trap state density, $D_{it}$, may be found by $qkT \eta_c = \frac{4Q_{nit}}{\tau_{ox}} \eta_c$ and applying Terman’s method which compares the difference between the ideal and trapped charge laden systems.
were measured to be 55 and 115 GHz, respectively. By em-
tron range between 0.9–6
ncreased band edge state density owing to the termina-
Figure 4 shows C-V characteristics measured at room-
temperature alongside the modeled ideal C-V curve for the
voltage comparison. The resultant interfacial density spectrum
is shown in the inset. The metal-insulator energy barrier and band-offset to AlN were taken as 0.72 and ∼2.5 eV,
respectively, based off Robertson’s work.11 Inaccuracies in
these values will lead to error in the energetic location of
the traps but does not interfere with the calculation of $D_n$. The
abrupt increase in $D_n$ near band edge may be due in part to
an increased band edge state density owing to the termina-
cation of the crystal periodicity at the surface.75 $D_n$ was found
to range between 0.9–6 × 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ (gray region).

Terman’s method implicitly probes interfacial charge states
which are below the ac perturbation frequency thus, fast states
are not accounted for. These “slow” states apparently do not impose deleterious effects on small signal fre-
quency performance as can be seen in Fig. 5. Small-signal
S-parameter characteristics were taken at the bias point that
yielded maximum $g_m$. Extrinsic values of unity current gain
frequency ($f_t$) and maximum frequency of operation ($f_{\text{max}}$)
were measured to be 55 and 115 GHz, respectively. By em-
ploying the ColdFET and standard Y-subtraction technique,18
pad parasitics were modeled (table inset, Fig. 5) and the de-
embedded value of $f_t$ was determined to be 75 GHz.

AlN/GaN HEMTs employing a 6 nm thick ALD Ta$_2$O$_5$
film for gate current suppression have been reported. The
gate oxide enabled $V_{DS}$ biases up to 96 V before destructive
breakdown. Maximum current density of 1.37 A/mm and
extrinsic transconductance of 315 mS/mm was measured.
Respective small signal frequency performance of $f_t$ and $f_{\text{max}}$,
was obtained despite a relatively high $D_n$. With further optimization of heterostructure growth,
shorter gate lengths, and the usage of Ta$_2$O$_5$ thin films for
gate insulation and improved robustness, the efficacy of the

$$D_n = \frac{C_{\text{ox}}}{qkT} \frac{\partial \Delta V_{\text{GS}}}{\partial \eta},$$

where $\Delta V_{\text{GS}} = V_{\text{GS,meas}} - V_{\text{GS,ideal}}$ at common capacitance.

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