TS8GSSD25S-S
TS16GSSD25S-S/M
TS32GSSD25S-S/M
TS64GSSD25S-S/M
TS128GSSD25S-M

2.5” Solid State Disk

Description

Due to smaller size (fit the standard dimensions of 2.5” SATA Hard Disk Drives), huge capacity, high speed, and low power consumption, Solid State Disk is perfect replacement storage device for PCs, Laptops, gaming systems, and handheld devices.

Placement

Features

- RoHS compliant
- Fully compatible with devices and OS that support the SATA Ⅱ 3.0Gbps standard
- Non-volatile Flash Memory for outstanding data retention
- Built-in ECC (Error Correction Code) functionality and wear-leveling algorithm ensures highly reliable of data transfer
- Shock resistance

Dimensions

Side	Millimeters	Inches
A	100.00 ± 0.40	3.937 ± 0.016
B	69.85 ± 0.20	2.750 ± 0.008
C	9.50 ± 0.15	0.374 ± 0.004

TS8GSSD25S-S
TS16GSSD25S-S/M
TS32GSSD25S-S/M
TS64GSSD25S-S/M
TS128GSSD25S-M

2.5” Solid State Disk

Specifications

Physical Specification		
Form Factor		2.5-inch HDD
Storage Capacities		8 GB to 128 GB
Dimensions (mm)	**Length**	100.0 0 ± 0.40
	Width	69.85 ± 0.20
	Height	9.50 ± 0.15
Input Voltage		5V ± 5%
Weight		48 g
Connector		SATA 7+15 pins combo connector

Environmental Specifications	
Operating Temperature	0 ℃ to 70 ℃
Storage Temperature	- 40 ℃ to 85 ℃

Power Requirements			
Input Voltage		5V ± 5% @25℃	
Mode		**Max. (mA)**	**Max. (W)**
Power Consumption (8/16/32/64GB)	**Write**$_{(peak)}$	443.1	2.2
	Read$_{(peak)}$	392.1	1.9
	Idle$_{(peak)}$	136.2	0.6
Power Consumption (128GB)	**Write**$_{(peak)}$	509.5	2.5
	Read$_{(peak)}$	445.1	2.2
	Idle$_{(peak)}$	134.3	0.6

Reliability	
Data Reliability	Supports BCH ECC 8 bits in 512 bytes
Data Retention	10 years
MTBF	1,000,000 hours

Regulations	
Compliance	CE, FCC and BSMI

TS8GSSD25S-S
TS16GSSD25S-S/M
TS32GSSD25S-S/M
TS64GSSD25S-S/M
TS128GSSD25S-M

2.5” Solid State Disk

Performance				
Model P/N	**Read(MB/s)**	**Write(MB/s)**	**Random Read(MB/s)**	**Random Write(MB/s)**
TS8GSSD25S-S	136~172	96~105	92~95	28
TS16GSSD25S-M	148	50	90	15
TS16GSSD25S-S	139~172	105~148	94~109	28
TS32GSSD25S-M	123~148	60~85	82~93	19
TS32GSSD25S-S	135~159	105~136	92~99	28
TS64GSSD25S-M	148	92	93	19
TS64GSSD25S-S	163	142	100	28
TS128GSSD25S-M	163	92	92	21

Actual Capacity				
Model P/N	**User Max. LBA**	**Cylinder**	**Head**	**Sector**
TS8GSSD25S-S	15,621,984	15,498	16	63
TS16GSSD25S-M	31,277,056	16,383	16	63
TS16GSSD25S-S	31,277,056	16,383	16	63
TS32GSSD25S-M	62,586,880	16,383	16	63
TS32GSSD25S-S	62,586,880	16,383	16	63
TS64GSSD25S-M	125,206,528	16,383	16	63
TS64GSSD25S-S	125,206,528	16,383	16	63
TS128GSSD25S-M	250,445,824	16,383	16	63

Vibration	
Operating	3.0G, 5 - 800Hz
Non-Operating	3.0G, 5 - 800Hz

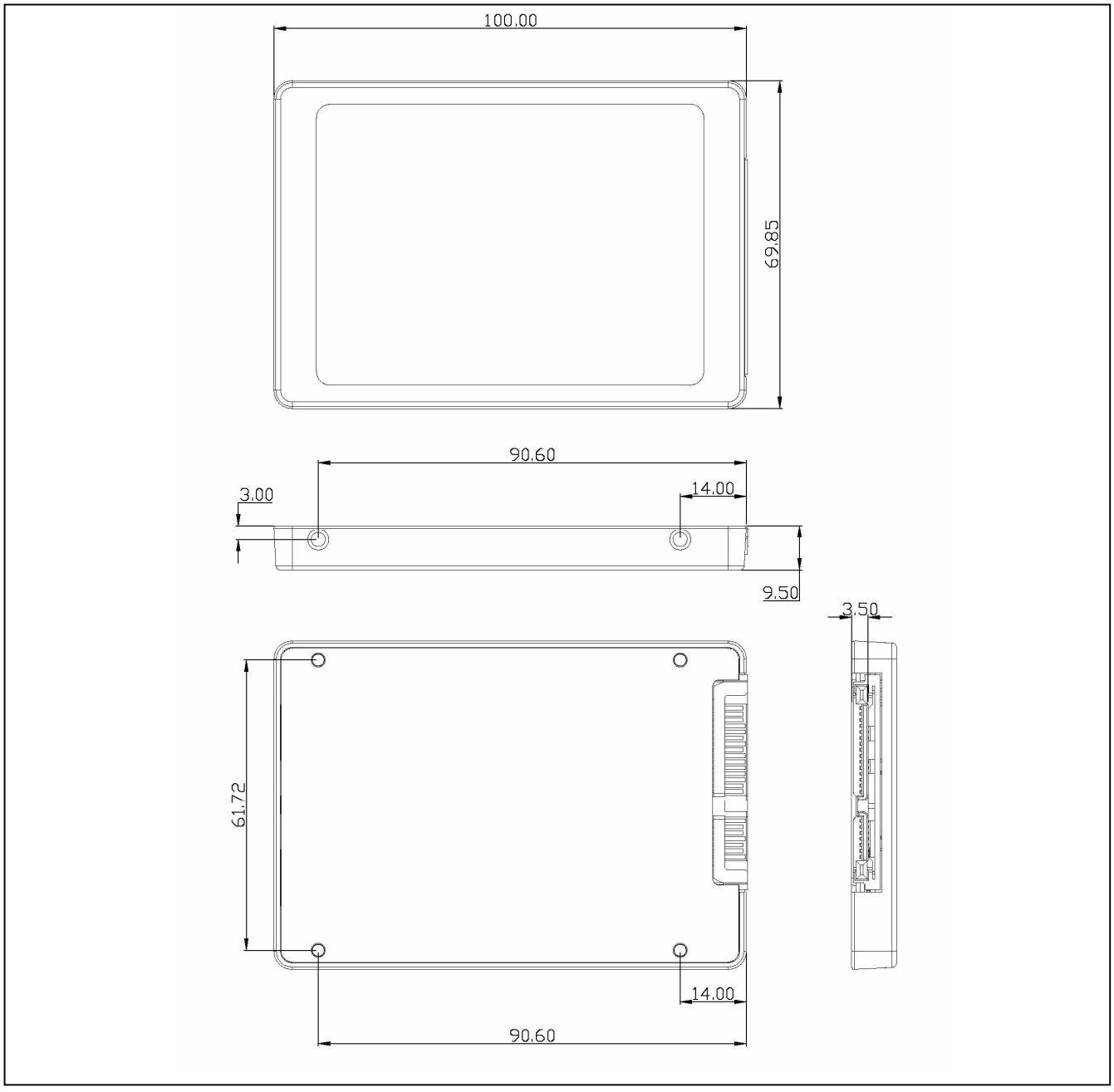
* Note: Reference to the IEC 60068-2-6 Testing procedures; Operating-Sine wave, 5-800Hz/1 oct., 1.5mm, 3g, 0.5 hr./axis, total 1.5 hrs.

Shock	
Operating	1500G, 0.5ms
Non-Operating	1500G, 0.5ms

* Note: Reference to the IEC 60068-2-27 Testing procedures; Operating-Half-sine wave, 1500g, 0.5ms, 3 times/dir., total 18 times.

Package Dimensions

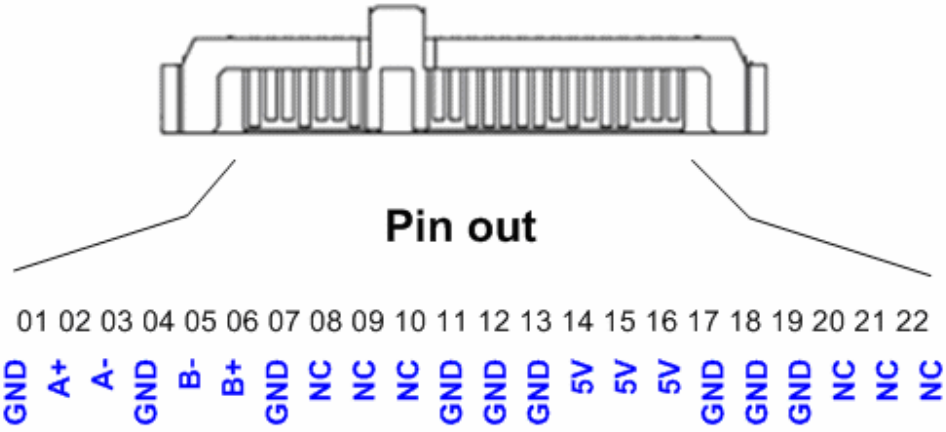
Below figure illustrates the Transcend 2.5” SATA Solid State Disk. All dimensions are in mm.



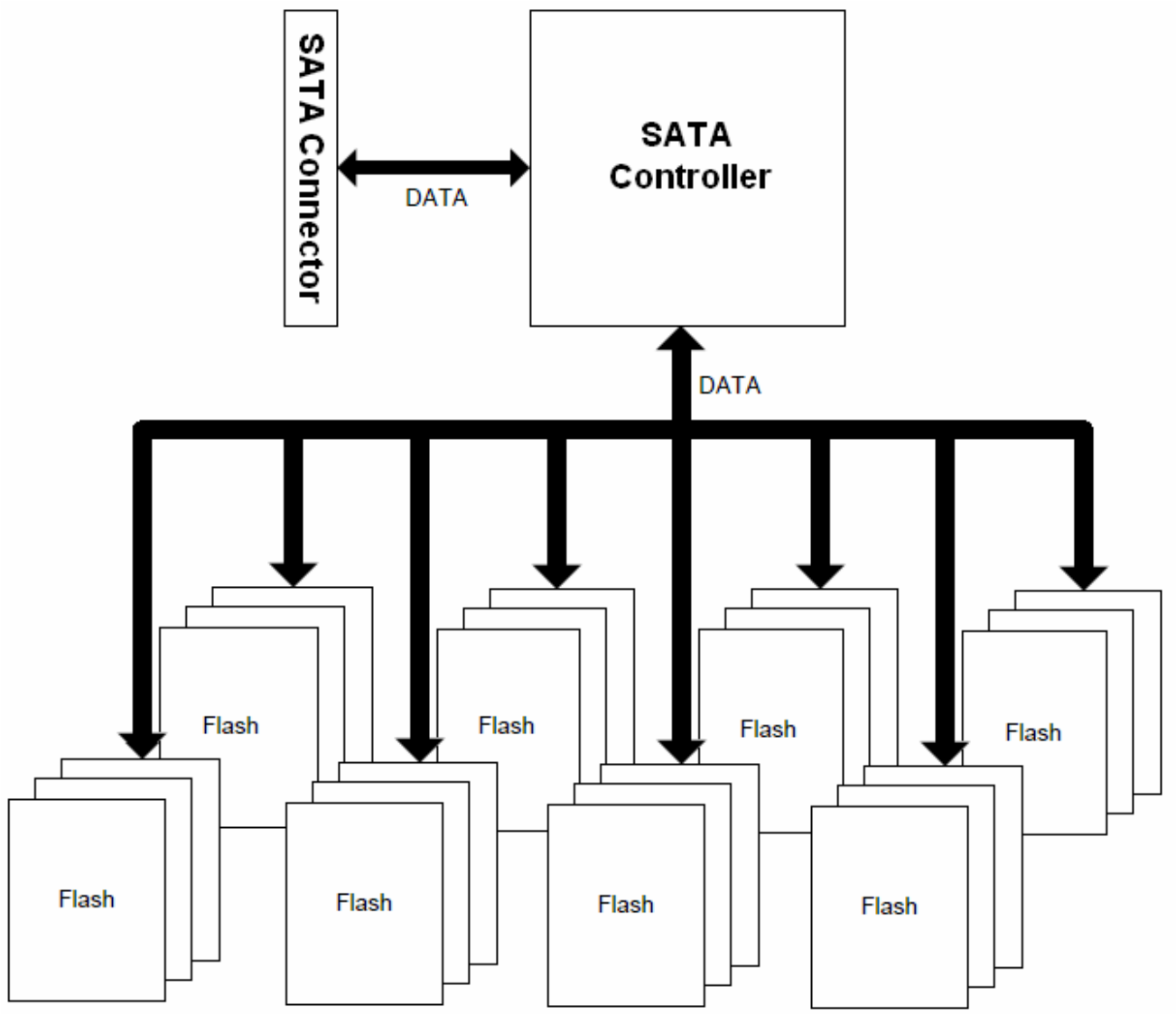
Pin Assignments

Pin No.	Pin Name	Pin No.	Pin Name
01	GND	02	A+
03	A-	04	GND
05	B-	06	B+
07	GND	08	NC
09	NC	10	NC
11	GND	12	GND
13	GND	14	5V
15	5V	16	5V
17	GND	18	GND
19	GND	20	NC
21	NC	22	NC

Pin Layout



Block Diagram



Reliability

Wear-Leveling algorithm

The controller supports static/dynamic wear leveling. When the host writes data, the controller will find and use the block with the lowest erase count among the free blocks. This is known as dynamic wear leveling. When the free blocks' erase count is higher than the data blocks', it will activate the static wear leveling, replacing the not so frequently used user blocks with the high erase count free blocks.

ECC algorithm

The controller use BCH8 ECC algorithm per 512 bytes. BCH8 can correct up to 8 random error bits within 512 data bytes.

Bad-block management

When the flash encounters ECC failed, program fail or erase fail, the controller will mark the block as bad block to prevent the used of this block and caused data lost later on.

SATA Interface

Out of bank signaling

There shall be three Out Of Band (OOB) signals used/detected by the Phy: COMRESET, COMINIT, and COMWAKE. COMINIT, COMRESET and COMWAKE OOB signaling shall be achieved by transmission of either a burst of four Gen1 $ALIGN_P$ primitives or a burst composed of four Gen1 Dwords with each Dword composed of four D24.3 characters, each burst having a duration of 160 UI_{OOB}. Each burst is followed by idle periods (at common-mode levels), having durations as depicted in Figure 4 and Table 2.

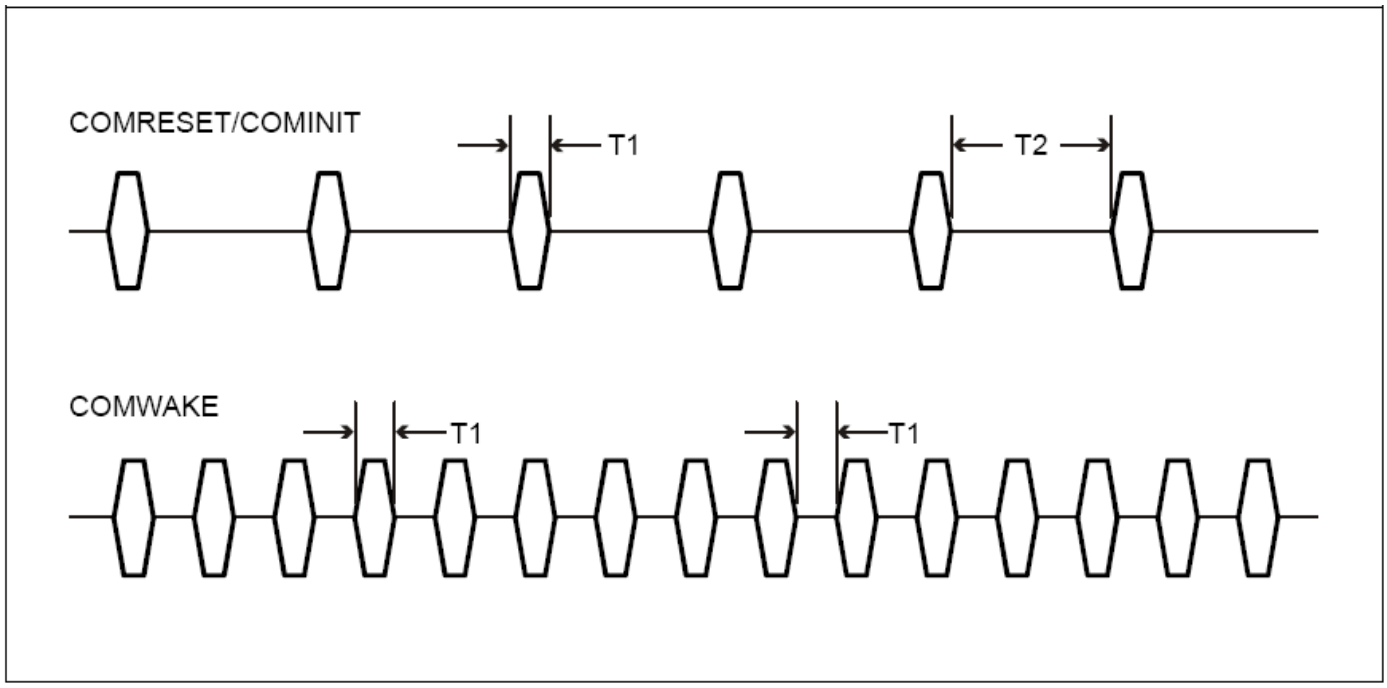


Figure 4 : OOB signals

Time	Value
T1	160 UI_{oob} (106.7 ns nominal)
T2	480 UI_{oob} (320 ns nominal)

Table 2 : OOB signal times

COMRESET

COMRESET always originates from the host controller, and forces a hardware reset in the device. It is indicated by transmitting bursts of data separated by an idle bus condition. The OOB COMRESET signal shall consist of no less than six data bursts, including inter-burst temporal spacing. The COMRESET signal shall be:

1) Sustained/continued uninterrupted as long as the system hard reset is asserted, or

2) Started during the system hardware reset and ended some time after the negation of system hardware reset, or

3) Transmitted immediately following the negation of the system hardware reset signal.

The host controller shall ignore any signal received from the device from the assertion of the hardware reset signal until the COMRESET signal is transmitted. Each burst shall be 160 Gen1 UI’s long (106.7 ns) and each inter-burst idle state shall be 480 Gen1 UI’s long (320 ns). A COMRESET detector looksfor four consecutive bursts with 320 ns spacing (nominal). Any spacing less than 175 ns or greater than 525 ns shall invalidate the COMRESET detector output. The COMRESET interface signal to the Phy layer shall initiate the Reset sequence shown in Figure 5 below. The interface shall be held inactive for at least 525 ns after the last burst to ensure far-end detector detects the negation properly.

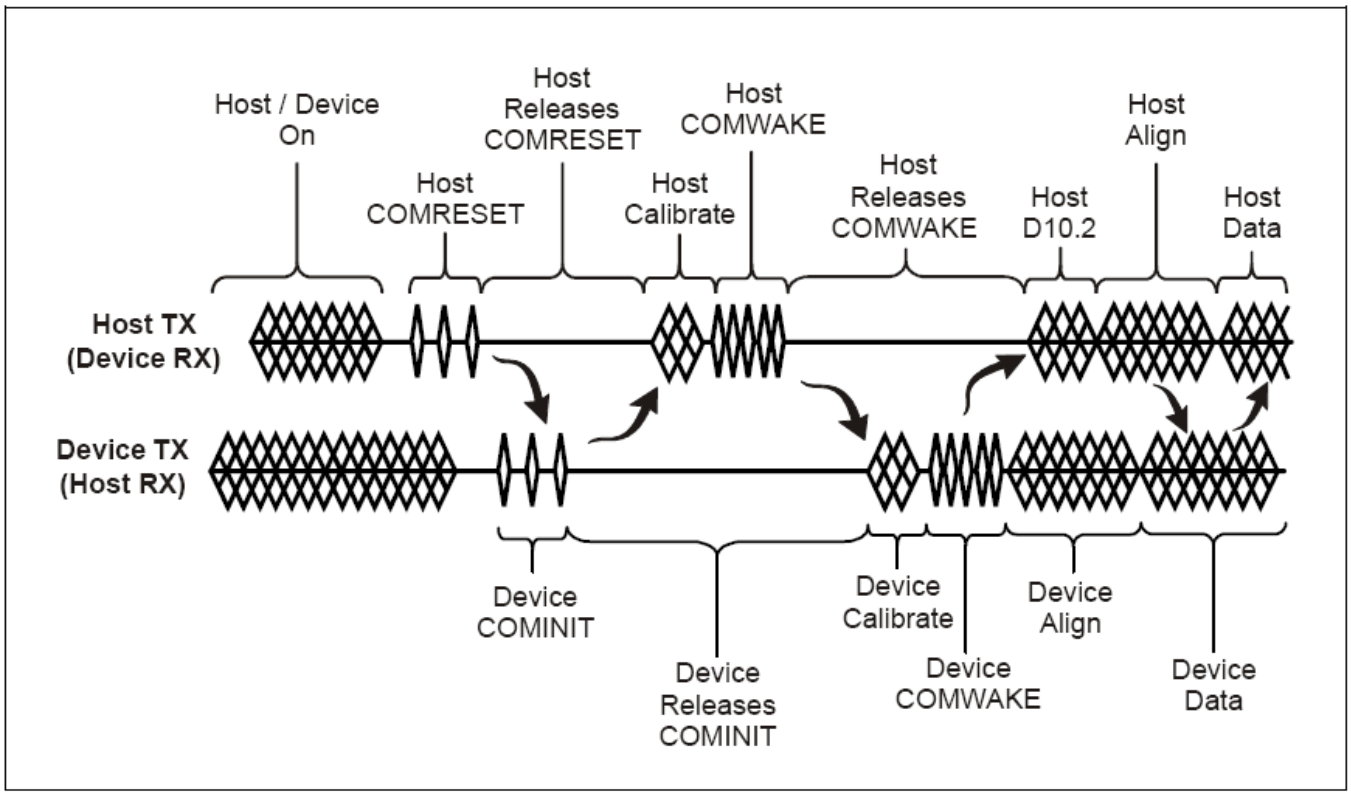


Figure 5 : comreset sequence

Description:

1. Host/device are powered and operating normally with some form of active communication.
2. Some condition in the host causes the host to issue COMRESET
3. Host releases COMRESET. Once the condition causing the COMRESET is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.
4. Device issues COMINIT – When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.
5. Host calibrates and issues a COMWAKE.
6. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP Dwords have been sent for 54.6us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device enters an error state.
7. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This ensures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer.
8. Device locks – the device locks to the ALIGN sequence and, when ready, sends SYNCP indicating it is ready to start normal operation.
9. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

COMINIT

COMINIT always originates from the drive and requests a communication initialization. It is electrically identical to the COMRESET signal except that it originates from the device and is sent to the host. It is used by the device to request a reset from the host in accordance to the sequence shown in Figure 6, below.

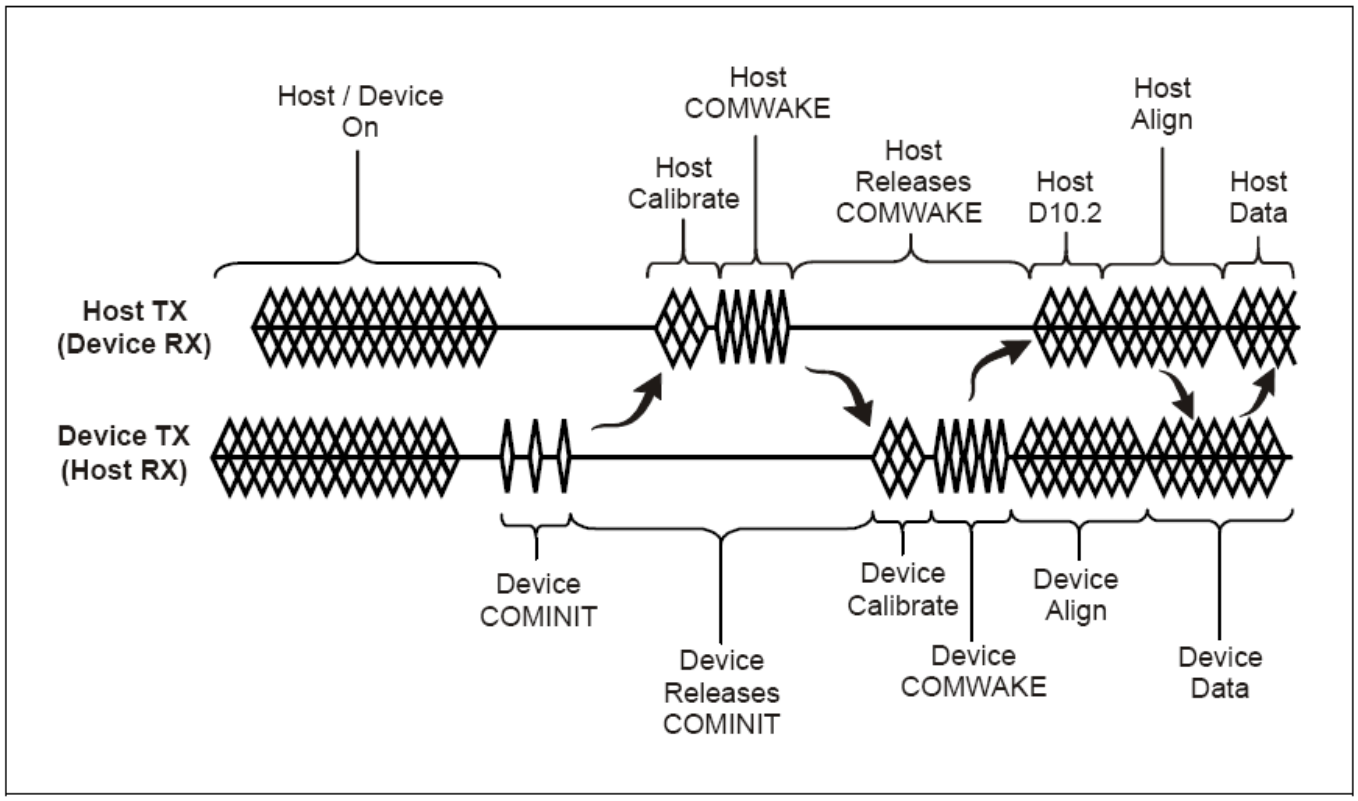


Figure 6 : cominit sequence

Description:

1. Host/device are powered and operating normally with some form of active communication.
2. Some condition in the device causes the device to issues a COMINIT
3. Host calibrates and issues a COMWAKE.
4. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP Dwords have been sent for 54.6 us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received

from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device enters an error state.

5. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6 us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This ensures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer. 6. Device locks – the device locks to the ALIGN sequence and, when ready, sends SYNCP indicating it is ready to start normal operation.

6. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

Power on sequence timing diagram

The following timing diagrams and descriptions are provided for clarity and are informative. The state diagrams provided in section 8.4 comprise the normative behavior specification and is the ultimate reference.

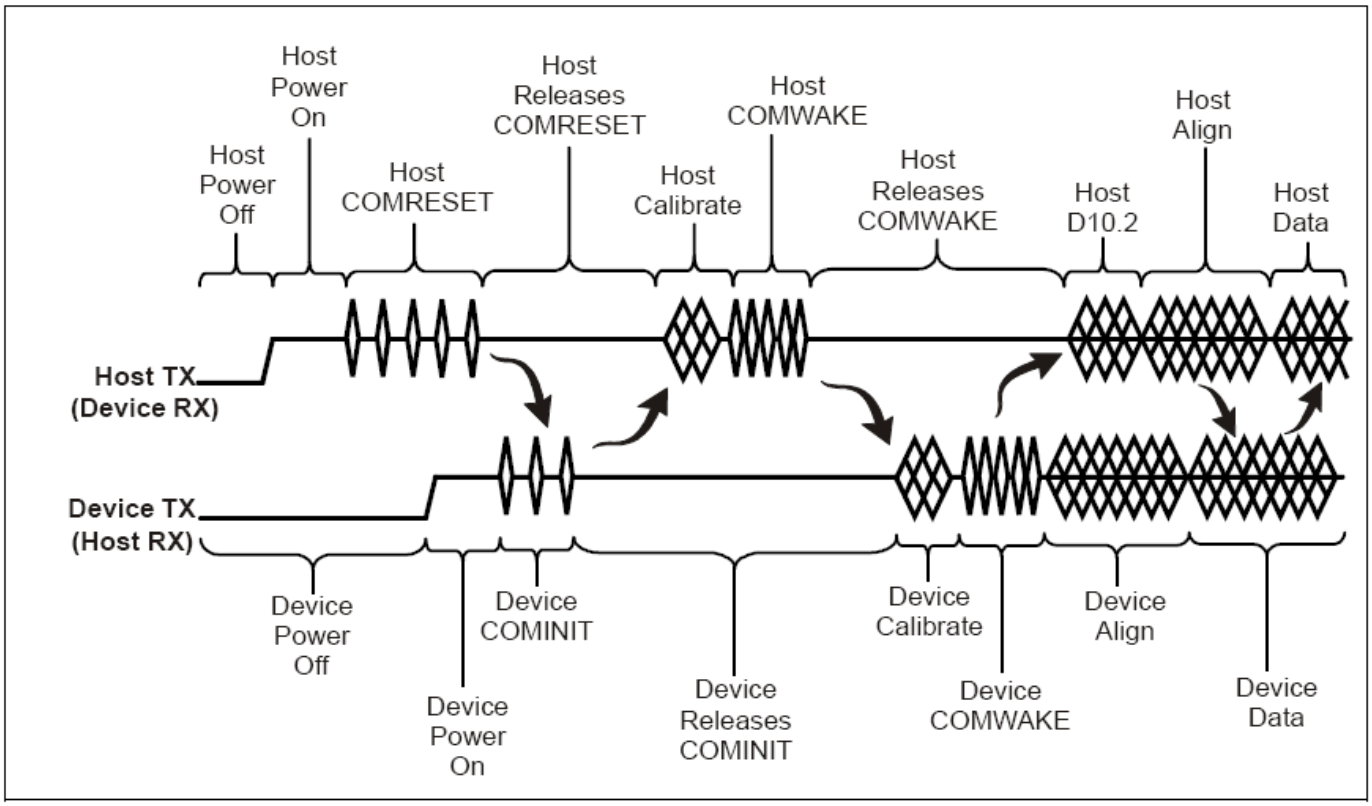


Figure 7 : power on sequence

Description:

1. Host/device power-off - Host and device power-off.

2. Power is applied - Host side signal conditioning pulls TX and RX pairs to neutral state (common mode voltage).

3. Host issues COMRESET

4. Host releases COMRESET. Once the power-on reset is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.

5. Device issues COMINIT – When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.

6. Host calibrates and issues a COMWAKE.

7. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After $ALIGN_P$ primitives have been sent for 54.6 us

(2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP primitives at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device shall enter an error state.

8. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6 us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This insures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer.

9. Device locks – the device locks to the ALIGN sequence and, when ready, sends the SYNCP primitive indicating it is ready to start normal operation.

10. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

ATA command register

This table with the following paragraphs summarizes the ATA command set.

Command Table

Command Name	Code	PARAMETERS USED					
		SC	SN	CY	DR	HD	FT
CHECK POWER MODE	E5h	X	X	X	O	X	X
EXECUTE DIAGNOSTICS	90h	X	X	X	O	X	X
FLUSH CACHE	E7h	X	X	X	O	O	X
IDENTIFY DEVICE	ECh	X	X	X	O	X	X
IDLE	E3h	O	X	X	O	X	X
IDLE IMMEDIATE	E1h	X	X	X	O	X	X
INITIALIZE DEVICE PARAMETERS	91h	O	X	X	O	O	X
READ DMA	C8h or C9h	O	O	O	O	O	X
READ MULTIPLE	C4h	O	O	O	O	O	X
READ SECTOR(S)	20h or 21h	O	O	O	O	O	X
READ VERIFY SECTOR(S)	40h or 41h	O	O	O	O	O	X
RECALIBRATE	10h	X	X	X	O	X	X
SECURITY DISABLE PASSWORD	F6h	X	X	X	O	X	X
SECURITY ERASE PREPARE	F3h	X	X	X	O	X	X
SECURITY ERASE UNIT	F4h	X	X	X	O	X	X
SECURITY FREEZE LOCK	F5h	X	X	X	O	X	X
SECURITY SET PASSWORD	F1h	X	X	X	O	X	X
SECURITY UNLOCK	F2h	X	X	X	O	X	X
SEEK	7xh	X	X	O	O	O	X
SET FEATURES	EFh	O	X	X	O	X	O
SET MULTIPLE MODE	C6h	O	X	X	O	X	X
SLEEP	E6h	X	X	X	O	X	X
SMART	B0h	X	X	O	O	X	O
STANDBY	E2h	X	X	X	O	X	X
STANDBY IMMEDIATE	E0h	X	X	X	O	X	X
WRITE DMA	CAh or CBh	O	O	O	O	O	X
WRITE MULTIPLE	C5h	O	O	O	O	O	X
WRITE SECTOR(S)	30h or 31h	O	O	O	O	O	X

Note:

O = Valid, X = Don't care

SC = Sector Count Register

SN = Sector Number Register

CY = Cylinder Low/High Register

DR = DEVICE SELECT Bit (DEVICE/HEAD Register Bit 4)

HD = HEAD SELECT Bit (DEVICE/HEAD Register Bit 3-0)

FT = Features Register

ATA Command Specifications

CHECK POWER MODE (E5h)

The host can use this command to determine the current power management mode.

EXECUTE DIAGNOSTICS (90h)

This command performs the internal diagnostic tests implemented by the drive.

FLUSH CACHE (E7h)

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

IDENTIFY DEVICE (ECh)

This commands read out 512Bytes of drive parameter information. Parameter Information consists of the arrangement and value as shown in the following table. This command enables the host to receive the Identify Drive Information from the device.

Identify Device Information Default Value

Word	Value	F/V	Description
			General configuration bit-significant information:
		F	15 0 = ATA device
		X	14-8 Retired
		F	7 1 = removable media device
0	0040h	X	6 Obsolete
		X	5-3 Retired
		F	2 Reserved
		X	1 Retired
		F	0 Reserved
1	XXXXh	X	Number of logical cylinders
2	C837h	V	Specific configuration
3	00XXh	X	Number of logical heads
4-5	XXXXh	X	Retired
6	XXXXh	X	Number of logical sector per logical track
7-8	XXXXh	V	Reserved for assignment by the CompactFlash_ Association
9	000Eh	X	Retired
10-19	XXXXh	F	Serial number (20 ASCII characters)
20-21	XXXXh	X	Retired
22	003Fh	X	Obsolete
23-26	XXXXh	F	Firmware revision (8 ASCII characters)
27-46	XXXXh	F	Model number (40 ASCII characters)
		F	15-8 80h
47	8000h	F	7-0 00h = Reserved
		F	01h = Maximum number of 1 sectors on READ/WRITE MULTIPLE commands
48	4000h	F	Reserved
			Capabilities
		F	15-14 Reserved for the IDENTIFY PACKET DEVICE command.
		F	13 1 = Standby timer values as specified in this standard are supported
			0 = Standby timer values shall be managed by the device
		F	12 Reserved for the IDENTIFY PACKET DEVICE command.
49	2F00h	F	11 1 = IORDY supported
			0 = IORDY may be supported
		F	10 1 = IORDY may be disabled
		F	9 1 = LBA supported
		F	8 1 = DMA supported.
		X	7-0 Retired
50	4000h		Capabilities

		F	15	Shall be cleared to zero.
		F	14	Shall be set to one.
		F	13-2	Reserved.
		X	1	Obsolete
		F	0	Shall be set to one to indicate a device specific Standby timer value minimum.
51	0280h	X	15-8	PIO data transfer cycle timing mode
			7-0	Reserved
52	0000h	X	Obsolete	
		F	15-3	Reserved
		F	2	1 = the fields reported in word 88 are valid 0 = the fields reported in word 88 are not valid
53	0007h	F	1	1 = the fields reported in words 70:64 are valid 0 = the fields reported in words 70:64 are not valid
		X	0	1 = the fields reported in words 58:54 are valid 0 = the fields reported in words 58:54 are not valid
54	XXXXh	X	Number of current cylinders	
55	00XXh	X	Number of current heads	
56	XXXXh	X	Number of current sector per track	
57-58	XXXXh	X	Current capacity in sectors	
		F	15-9	Reserved
59	0000h	V	8	1 = Multiple sector setting is valid
		V	7-0	xxh = Setting for number of sectors that shall be transferred per interrupt on R/W Multiple command
60-61	XXXXh	F	Total number of user addressable sectors	
62	0000h	X	Obsolete	
		F	15-11	Reserved
		V	10	1 = Multiword DMA mode 2 is selected 0 = Multiword DMA mode 2 is not selected
		V	9	1 = Multiword DMA mode 1 is selected 0 = Multiword DMA mode 1 is not selected
63	0007h	V	8	1 = Multiword DMA mode 0 is selected 0 = Multiword DMA mode 0 is not selected
		F	7-3	Reserved
		F	2	1 = Multiword DMA mode 2 and below are supported
		F	1	1 = Multiword DMA mode 1 and below are supported
		F	0	1 = Multiword DMA mode 0 is supported
		F	15-8	Reserved
64	0003h	F	7-0	Advanced PIO modes supported
65	0078h	F	Minimum Multiword DMA transfer cycle time per word	
66	0078h	F	Manufacturer’s recommended Multiword DMA transfer cycle time	
67	0078h	F	Minimum PIO transfer cycle time without flow control	
68	0078h	F	Minimum PIO transfer cycle time with IORDY flow control	

69-79	0000h	F		Reserved (for future command overlap and queuing)
80	01FEh			Major version number 0000h or FFFFh = device does not report version
		F	15	Reserved
		F	14	Reserved for ATA/ATAPI-14
		F	13	Reserved for ATA/ATAPI-13
		F	12	Reserved for ATA/ATAPI-12
		F	11	Reserved for ATA/ATAPI-11
		F	10	Reserved for ATA/ATAPI-10
		F	9	Reserved for ATA/ATAPI-9
		F	8	Reserved for ATA/ATAPI-8
		F	7	1 = supports ATA/ATAPI-7
		F	6	1 = supports ATA/ATAPI-6
		F	5	1 = supports ATA/ATAPI-5
		F	4	1 = supports ATA/ATAPI-4
		F	3	Obsolete
		X	2	Obsolete
		X	1	Obsolete
		F	0	Reserved
81	0021h	F		Minor version number
82	0068h			Command set supported.
		X	15	Obsolete
		F	14	1 = NOP command supported
		F	13	1 = READ BUFFER command supported
		F	12	1 = WRITE BUFFER command supported
		X	11	Obsolete
		F	10	1 = Host Protected Area feature set supported
		F	9	1 = DEVICE RESET command supported
		F	8	1 = SERVICE interrupt supported
		F	7	1 = release interrupt supported
		F	6	1 = look-ahead supported
		F	5	1 = write cache supported
		F	4	Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.
		F	3	1 = mandatory Power Management feature set supported
		F	2	1 = Removable Media feature set supported
		F	1	1 = Security Mode feature set supported
		F	0	1 = SMART feature set supported
83	5000h			Command sets supported.
		F	15	Shall be cleared to zero
		F	14	Shall be set to one
		F	13-9	Reserved
		F	8	1 = SET MAX security extension supported
		F	7	Reserved
		F	6	1 = SET FEATURES subcommand required to spinup after power-up
		F	5	1 = Power-Up In Standby feature set supported
		F	4	1 = Removable Media Status Notification feature set supported
		F	3	1 = Advanced Power Management feature set supported

		F	2	1 = CFA feature set supported
		F	1	1 = READ/WRITE DMA QUEUED supported
		F	0	1 = DOWNLOAD MICROCODE command supported
				Command set/feature supported extension.
		F	15	Shall be cleared to zero
		F	14	Shall be set to one
84	4000h	F	13-2	Reserved
		F	1	1 = SMART self-test supported
		F	0	1 = SMART error logging supported
				Command set/feature enabled.
		X	15	Obsolete
		F	14	1 = NOP command enabled
		F	13	1 = READ BUFFER command enabled
		F	12	1 = WRITE BUFFER command enabled
		X	11	Obsolete
		V	10	1 = Host Protected Area feature set enabled
		F	9	1 = DEVICE RESET command enabled
85	0008h	V	8	1 = SERVICE interrupt enabled
		V	7	1 = release interrupt enabled
		V	6	1 = look-ahead enabled
		V	5	1 = write cache enabled
		F	4	Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.
		F	3	1 = Power Management feature set enabled
		F	2	1 = Removable Media feature set enabled
		V	1	1 = Security Mode feature set enabled
		V	0	1 = SMART feature set enabled
				Command set/feature enabled.
		F	15-9	Reserved
		F	8	1 = SET MAX security extension enabled by SET MAX SET PASSWORD
		F	7	See Address Offset Reserved Area Boot, INCITS TR27:2001
86	5000h	F	6	1 = SET FEATURES subcommand required to spin-up after power-up
		V	5	1 = Power-Up In Standby feature set enabled
		V	4	1 = Removable Media Status Notification feature set enabled
		V	3-1	1 = Advanced Power Management feature set enabled
		F	0	1 = DOWNLOAD MICROCODE command supported
				Command set/feature default.
		F	15	Shall be cleared to zero
		F	14	Shall be set to one
87	4000h	F	13-2	Reserved
		F	1	1 = SMART self-test supported
		F	0	1 = SMART error logging supported
			15-13	Reserved
		V	12	1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected
88	203Fh	V	11	1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected
		V	10	1 = Ultra DMA mode 2 is selected

				0 = Ultra DMA mode 2 is not selected
		V	9	1 = Ultra DMA mode 1 is selected
				0 = Ultra DMA mode 1 is not selected
		V	8	1 = Ultra DMA mode 0 is selected
				0 = Ultra DMA mode 0 is not selected
		F	7-5	Reserved
		F	4	1 = Ultra DMA mode 4 and below are supported
		F	3	1 = Ultra DMA mode 3 and below are supported
		F	2	1 = Ultra DMA mode 2 and below are supported
		F	1	1 = Ultra DMA mode 1 and below are supported
		F	0	1 = Ultra DMA mode 0 is supported
89	0000h	F		Time required for security erase unit completion
90	0000h	F		Time required for Enhanced security erase completion
91	0000h	V		Current advanced power management value
92	0000h	V		Master Password Revision Code
93	0000h	X		Hardware reset result
94-126	0000h	V		Reserved
127	0000h			Removable Media Status Notification feature set support
		F	15-2	Reserved
		F	1-0	00 = Removable Media Status Notification feature set not supported
				01 = Removable Media Status Notification feature supported
				10 = Reserved
				11 = Reserved
128	0001h			Security status
		F	15-9	Reserved
		V	8	Security level 0 = High, 1 = Maximum
		F	7-6	Reserved
		F	5	1 = Enhanced security erase supported
		V	4	1 = Security count expired
		V	3	1 = Security frozen
		V	2	1 = Security locked
		V	1	1 = Security enabled
		F	0	1 = Security supported
129-159	0000h	X		Vendor specific
160-254	0000h	X		Reserved
255	0000h	X		Integrity word
			15-8	Checksum
			7-0	Signature

Key:

F/V = Fixed/variable content

F = the content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.

V = the contents of the word is variable and may change depending on the state of the device or the commands executed by

the device.
X = the content of the word may be fixed or variable.

IDLE (E3h)

This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power mode is disabled.

IDLE IMMEDIATE (E1h)

This command causes the device to set BSY, enter the Idle(Read) mode, clear BSY and generate an interrupt.

INITIALIZE DEVICE PARAMETERS (91h)

This command enables the host to set the number of sectors per track and the number of tracks per heads.

READ DMA (C8h)

Read data from sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value. A sector count of zero requests 256 sectors.

READ MULTIPLE (C4h)

This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

READ SECTOR(S) (20h/21h)

This command reads 1 to 256 sectors as specified in the Sector Count register from sectors which is set by Sector number register. A sector count of 0 requests 256 sectors. The transfer beings specified in the Sector Number register.

READ VERIFY SECTOR(S) (40h/41h)

This command verifies one or more sectors on the drive by transferring data from the flash media to the data buffer in the drive and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

RECALIBRATE (10h)

The current drive performs no processing if it receives this command. It is supported for backward compatibility with previous devices.

SECURITY DISABLE PASSWORD (F6h)

Disables any previously set user password and cancels the lock. The host transfers 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY ERASE PREPARE (F3h)

This command shall be issued immediately before the Security Erase Unit command to enable erasing and unlocking. This command prevents accidental loss of data on the drive.

SECURITY ERASE UNIT (F4h)

The host uses this command to transfer 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive deletes user data, disables the user password, and cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY FREEZE LOCK (F5h)

Causes the drive to enter Frozen mode. Once this command has been executed, the following commands to update a lock result in the Aborted Command error:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

The drive exits from Frozen mode upon a power-off or hard reset. If the SECURITY FREEZE LOCK command is issued when the drive is placed in Frozen mode, the drive executes the command, staying in Frozen mode.

SECURITY SET PASSWORD (F1h)

This command set user password or master password. The host outputs sector data with PIO data-out protocol to indicate the information defined in the following table.

Security set Password data content

Word	Content		
0	Control word		
	Bit 0	Identifier	0=set user password
			1=set master password
	Bits 1-7	Reserved	
	Bit 8	Security level	0=High
			1=Maximum
	Bits 9-15	Reserved	
1-16	Password (32 bytes)		
17-255	Reserved		

SECURITY UNLOCK (F2h)

This command disable LOCKED MODE of the device. This command transfers 512 bytes of data from the host with PIO data-out protocol. The following table defines the content of this information.

Security Unlock information

Word	Content		
0	Control word		
	Bit 0	Identifier	0=compare user password 1=compare master password
	Bits 1-15	Reserved	
1-16	Password (32 bytes)		
17-255	Reserved		

SEEK (7xh)

This command is effectively a NOP command to the device although it does perform a range check.

SET FEATURES (EFh)

This command set parameter to Features register and set drive’s operation. For transfer mode, parameter is set to Sector Count register. This command is used by the host to establish or select certain features.

Features register Value and settable operating mode

Value	Function
02h	Enable write cache
03h	Set transfer mode based on value in Sector Count register.
55h	Disable read look-ahead feature
82h	Disable write cache
AAh	Enable read look-ahead feature

SET MULTIPLE MODE (C6h)

This command enables the device to perform READ MULTIPLE and WRITE MULTIPLE operations and establishes the block count for these commands.

SLEEP (E6h)

This command causes the device to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

SMART Function Set (B0h)

Performs different processing required for predicting device failures, according to the subcommand specified in the

Features register. If the Features register contains an unsupported value, the Aborted Command error is returned. If the SMART function is disabled, any subcommand other than SMART ENABLE OPERATIONS results in the Aborted Command error.

SMART Sub Command Set

Value	Function
D0h	Read Data
D1h	Read Attribute Thresholds
D2h	Enable/Disable Autosave
D3h	Save Attribute Values
D8h	Enable Operations
D9h	Disable Operations
DAh	Return Status

SMART ID List

ID(Hex)	Description	Reference
0C	Power Cycle Count	Support
09	Power On Hours Count	Not Support
C2	Temperature	Not Support
E5	Halt System ID, Flash ID	Table 1
E8	Firmware version information	Table 2
E9	ECC Fail Record	Table 3
EA	Average Erase Count, Max Erase Count	Table 4
EB	Good Block Count, System Block Count	Table 5
EC~EF	Reserved	
F1~FF	Reserved	

Individual Attribute Data structure

Byte	Description
0	Attribute ID
1	Status Flag (0x0002)
2	
3	Attribute Value (0x64)

4~11	Vendor Specific

Table 1

Byte	Description
0	Halt System ID
1	Flash ID (byte 1)
2	Flash ID (byte 2)
3	Flash ID (byte 3)
4	Flash ID (byte 4)
5	Flash ID (byte 5)
6	Flash ID (byte 6)
7	Flash ID (byte 7)

Table 2

Byte	Description
0	Year (High Byte, ASCII)
1	Year (Low Byte, ASCII)
2	Month (High Byte, ASCII)
3	Month (Low Byte, ASCII)
4	Day (High Byte, ASCII)
5	Day (Low Byte, ASCII)
6	Channels (binary)
7	Banks (binary)

Table 3

Byte	Description
0	ECC fail number
1	Row address 3
2	Row address 2
3	Row address 1
4	Channel number of last ECC fail
5	Bank number of last ECC fail
6~7	Reserved

Table 4

Byte	Description
0	Average Erase Count (High Byte)
1	Average Erase Count
2	Average Erase Count (Low Byte)
3	Max Erase Count (High Byte)
4	Max Erase Count
5	Max Erase Count (Low Byte)
6~7	Reserved

Table 5

Byte	Description
0	Good Block Count (High Byte)
1	Good Block Count
2	Good Block Count (Low Byte)
3	System(Free) Block Count (High Byte)
4	System(Free) Block Count (Low Byte)
5	Reserved
6	Reserved
7	Reserved

STANDBY (E2h)

This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately.

STANDBY IMMEDIATE (E0h)

This command causes the drive to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately.

WRITE DMA (CAh)

Write data to sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value.

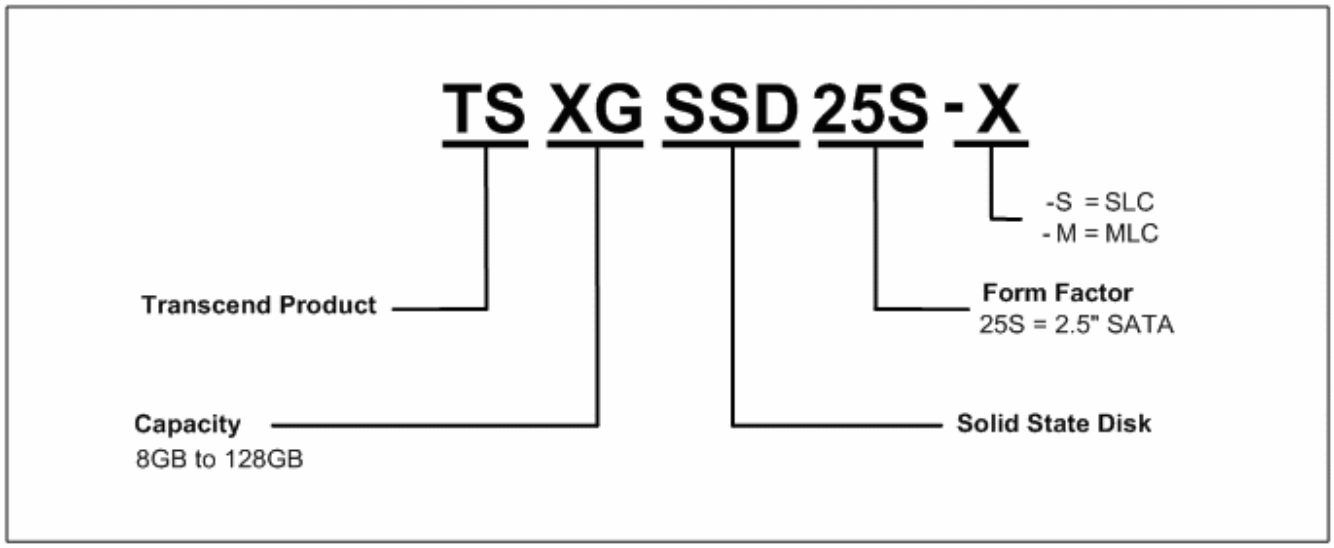
WRITE MULTIPLE (C5h)

This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

WRITE SECTOR(S) (30h/31h)

Write data to a specified number of sectors (1 to 256, as specified with the Sector Count register) from the specified address. Specify “00h” to write 256 sectors.

Ordering Information



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