

Designing Complex Software

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Since 1978, the goal of the Software Cost Reduction (SCR) project has been to demonstrate the effectiveness of certain software engineering techniques for developing complex software. The application is the redevelopment of the operational flight program for the A-7E aircraft. Also since then, the Software Technology Evaluation (STE) project has been monitoring SCR project activity in order to provide an objective evaluation of the SCR methodology. SCR project activity data are collected from SCR personnel on a weekly basis. Over 55000 hours of SCR design, code, test, and other activity data have been captured and recorded in a computer data base. Analyses of SCR module design data show that there are parameters that can be used to characterize and predict design progress. One example is the ratio between cumulative design discussing activities and cumulative design creating activities. This ratio is referred to as the Progress Indicator Ratio (PIR) and seems to be an accurate metric for design completeness. This and other results suggest that discussion activity among software engineers may play a major role in the software design process and may be a leading indicator of design activity progress.

1. INTRODUCTION

This paper presents the results of an investigation of design activities of the software engineers working on the Software Cost Reduction (SCR) project. One purpose of this study is to offer insights into understanding the design process of complex software. A second purpose is to identify parameters that characterize and predict design progress. The data analyses suggest that at least one parameter does characterize and predict design progress under the SCR approach.

1.1 The Software Cost Reduction Project

Since 1978, the Naval Research Laboratory in cooperation with the Naval Weapons Center has been redevelop-

ing version 2 of the operational flight program for the A-7E aircraft [4]. Software engineering techniques such as formal requirements specification, information hiding [10], abstract interfaces [11], and cooperating sequential processes [5] are being used. This effort is referred to as the Software Cost Reduction project.

The goals of the SCR project are to demonstrate the feasibility of using selected software engineering techniques in developing complex, real-time software, and to provide a model for software design. The claimed advantage of the selected software engineering techniques is that they can facilitate the development of easy-to-change software. A complete discussion of the project's software requirements is provided by Heninger, et al. [7]. For a detailed description of the module design structure, the reader is referred to Britton and Parnas [2].

1.2 The Software Technology Evaluation Project

The goal of the Software Technology Evaluation (STE) project is to evaluate alternative software development technologies. The approach is to monitor, evaluate, and compare software development technologies used in different software projects. The monitoring and evaluating processes consist of goal-directed data collection and analyses techniques [1]. One of the tasks of the STE project is to provide the basis for an objective evaluation of the methodology used in the SCR project. The two projects are, however, separate research investigations each with its own goals, staff, and funding.

2. DATA COLLECTION

Since 1978, all SCR project engineers have been required to submit weekly reports on their project activity hours. The activity data are collected on a form called the Weekly Activity Report, the current version of which is presented in Chart 1. The boxes on the form represent different project activities.

A submitted report is usually rather sparse; typically, it has only a few boxes marked with hours spent on

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SCR Project: Weekly Activity Report

Your name: _____

Date: Friday

| ACTIVITY AREA | ACTIVITY HOURS | | | | | | | | | | | | | |
|----------------------------|----------------|------------|----------------|------------------|-------------|------------|----------------|--------------|------------|----------------|--------------------|-------------|------------|-------------------|
| | Design | | | | Pseudo Code | | | EC/C/TC Code | | | | Test | | |
| | Creating | Discussing | Peer Reviewing | Formal Reviewing | Creating | Discussing | Peer Reviewing | Creating | Discussing | Peer Reviewing | Programmer Testing | Preparation | Conducting | Reviewing Results |
| Software Structures | | | | | | | | | | | | | | |
| Module Guide | | | | | | | | | | | | | | |
| Uses Hierarchy | | | | | | | | | | | | | | |
| Software Modules | | | | | | | | | | | | | | |
| Hardware Hiding | | | | | | | | | | | | | | |
| Extended Computer | | | | | | | | | | | | | | |
| _____ | | | | | | | | | | | | | | |
| _____ | | | | | | | | | | | | | | |
| Device Interface | | | | | | | | | | | | | | |
| _____ | | | | | | | | | | | | | | |
| _____ | | | | | | | | | | | | | | |
| Behavior Hiding | | | | | | | | | | | | | | |
| Function Driver | | | | | | | | | | | | | | |
| _____ | | | | | | | | | | | | | | |
| _____ | | | | | | | | | | | | | | |
| Shared Services | | | | | | | | | | | | | | |
| _____ | | | | | | | | | | | | | | |
| _____ | | | | | | | | | | | | | | |
| Software Decision | | | | | | | | | | | | | | |
| Application Data Types .. | | | | | | | | | | | | | | |
| _____ | | | | | | | | | | | | | | |
| Physical Model | | | | | | | | | | | | | | |
| _____ | | | | | | | | | | | | | | |
| Filter Behavior | | | | | | | | | | | | | | |
| _____ | | | | | | | | | | | | | | |
| _____ | | | | | | | | | | | | | | |
| Date Banker | | | | | | | | | | | | | | |
| _____ | | | | | | | | | | | | | | |
| _____ | | | | | | | | | | | | | | |
| System Generation | | | | | | | | | | | | | | |
| _____ | | | | | | | | | | | | | | |
| _____ | | | | | | | | | | | | | | |
| Software Utility | | | | | | | | | | | | | | |
| _____ | | | | | | | | | | | | | | |

(See reverse side)

Chart 1. Weekly activity report form.

| ACTIVITY AREA | ACTIVITY HOURS | | | | | | | | | | | | | |
|-------------------------|----------------|------------|----------------|------------------|-------------|------------|----------------|--------------|------------|----------------|--------------------|-------------|------------|-------------------|
| | Design | | | | Pseudo Code | | | EC/C/TC Code | | | | Test | | |
| | Creating | Discussing | Peer Reviewing | Formal Reviewing | Creating | Discussing | Peer Reviewing | Creating | Discussing | Peer Reviewing | Programmer Testing | Preparation | Conducting | Reviewing Results |
| Software Testing | | | | | | | | | | | | | | |
| General | | | | | | | | | | | | | | |
| Subset | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |

| MISCELLANEOUS ACTIVITY | HOURS |
|--------------------------------------|-------|
| Project Control | |
| Software Requirements Document | |
| Travel | |
| Technology Transfer | |
| Other: | |
| | |
| | |
| | |
| | |
| Non SCR (Optional): | |
| | |
| | |

project activities during the week. A copy of a completed report form is presented in Chart 2. Once a weekly activity report is given to STE project personnel, it is validated and entered into a computer data base. An instruction sheet explaining how to report weekly activity is provided to each SCR engineer.

2.1 Module Development Activities

The front page of the report form is primarily used to record hours spent on module development activity, where module means information hiding module [10]. As can be seen in Chart 1, SCR development activity

Chart 1. (continued).

hours are captured for each engineer by specific module within the hierarchy (e.g., Device Interface), and by design, code, and test categories. Space is provided for project personnel to supply the names of the modules below the first two levels.

The primary product of design activity is the development of a module interface specification. A typical interface specification for the Device Interface module [8] is presented in Chart 3. Design activity is reported as hours devoted to design creating, design discussing,

SCR Project: Weekly Activity Report

Your name: _____

Date: Friday, 02/10/84

| ACTIVITY AREA | ACTIVITY HOURS | | | | | | | | | | | | |
|----------------------------|----------------|------------|----------------|------------------|-------------|------------|----------------|--------------|------------|----------------|--------------------|-------------|------------|
| | Design | | | | Pseudo Code | | | EC/C/TC Code | | | | Test | |
| | Creating | Discussing | Peer Reviewing | Formal Reviewing | Creating | Discussing | Peer Reviewing | Creating | Discussing | Peer Reviewing | Programmer Testing | Preparation | Conducting |
| Software Structures | | | | | | | | | | | | | |
| Module Guide | | | | | | | | | | | | | |
| Uses Hierarchy | | | | | | | | | | | | | |
| Software Modules | | | | | | | | | | | | | |
| Hardware Hiding | | | | | | | | | | | | | |
| Extended Computer | | | 10 | | | | | | | | | | |
| SEQ | | | 2 | | | | | | | | | | |
| VM | | | 2 | | | | | | | | | | |
| Device Interface | | | | | | | | | | | | | |
| Behavior Hiding | | | | | | | | | | | | | |
| Function Driver | 20 | | | | | | | | | | | | |
| Shared Services | 4 | | | | | | | | | | | | |
| Software Decision | | | | | | | | | | | | | |
| Application Data Types .. | | | | | | | | | | | | | |
| Physical Model | | | | | | | | | | | | | |
| Filter Behavior | | | | | | | | | | | | | |
| Data Banker | | | | | | | | | | | | | |
| System Generation | | | | | | | | | | | | | |
| Software Utility | | | | | | | | | | | | | |

(See reverse side)

Chart 2. Completed weekly activity form.

| ACTIVITY AREA | ACTIVITY HOURS | | | | | | | | | | | | | |
|-------------------------|----------------|------------|----------------|------------------|-------------|------------|----------------|--------------|------------|----------------|--------------------|-------------|------------|-------------------|
| | Design | | | | Pseudo Code | | | EC/C/TC Code | | | | Test | | |
| | Creating | Discussing | Peer Reviewing | Formal Reviewing | Creating | Discussing | Peer Reviewing | Creating | Discussing | Peer Reviewing | Programmer Testing | Preparation | Conducting | Reviewing Results |
| Software Testing | | | | | | | | | | | | | | |
| General | | | | | | | | | | | | | | |
| Subset | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |

| MISCELLANEOUS ACTIVITY | HOURS |
|--------------------------------------|-------|
| Project Control | 5 |
| Software Requirements Document | |
| Travel | |
| Technology Transfer | |
| Other: | |
| | |
| | |
| | |
| | |
| Non SCR (Optional): | |
| | |
| | |

design peer reviewing, and design formal reviewing activities. *Design creating* activity is time devoted to thinking about a design including redesigning or documenting. *Design discussing* activity is time devoted to discussing design issues via a computer message or directly with a colleague to assist with the design. *Design peer reviewing* activity is time devoted to reading or commenting (informally) on design documentation produced by another project member in order to assist with the design. *Design formal reviewing* activity is time spent in a formal design review, typically at the Naval Weapons Center, which maintains the current operational flight program.

Chart 2. (continued).

Coding activity is reported as hours devoted to pseudo code, Extended Computer code, ¹ C code, and TC code² activities. Pseudo code activity is further reported as hours devoted to code creating, code discussing, and code peer reviewing activities. EC code, C code, and

¹ The Extended Computer is one of the modules of the program. EC code consists of invocations of programs on this module's interface.

² TC code is the assembly language code for the IBM System 4 PI model TC-2 computer. The operational flight program runs on this machine.

CHAPTER 23

DI.WOG: WEIGHT ON GEAR SENSOR

1. Introduction

The weight on gear device is a sensor that detects whether or not the aircraft is resting on its landing gear. This data can be used to infer whether or not the aircraft is airborne.

2. Interface overview

2.1. ACCESS PROGRAM TABLE

| <i>Program</i> | <i>Parameters</i> | <i>Description</i> | <i>Undesired events</i> |
|--------------------|-------------------|--------------------|-------------------------|
| +G_WEIGHT_ON_GEAR+ | p1: boolean; O | !+WOG+! | None |

2.2. EVENTS SIGNALLED

@T/@F/=T/=F(!+WOG+!)

3. Local type definitions None.

4. Dictionary

!+WOG+! \$true\$ iff weight on landing gear detected.

5. Undesired event dictionary None.

6. System generation parameters None.

DI.WOG

Chart 3. An interface specification for the device interface module.

TC code activities are reported as hours devoted to code creating, code discussing, code peer reviewing, and code programmer testing activities. *Code creating*, *code discussing*, and *code peer reviewing* activities have definitions similar to their design counterparts. *Code programmer testing* activity is time devoted by programmers to computer-based evaluation of their own code to convince themselves of its correctness.

Test activity is reported as hours devoted to test preparation, test conducting, and test reviewing results

activities. *Test preparation* activity is time devoted to creating, discussing, and reviewing plans and procedures for computer-based testing of a module prior to formal subset testing. *Test conducting* activity is time devoted to set up and execution of module test procedures on a computer. *Test reviewing results* activity is time devoted to analyzing, discussing, and documenting results of a module test.

2.2 Other Activities

The back page of the form is used to record hours spent on software testing and miscellaneous activities. *Soft-*

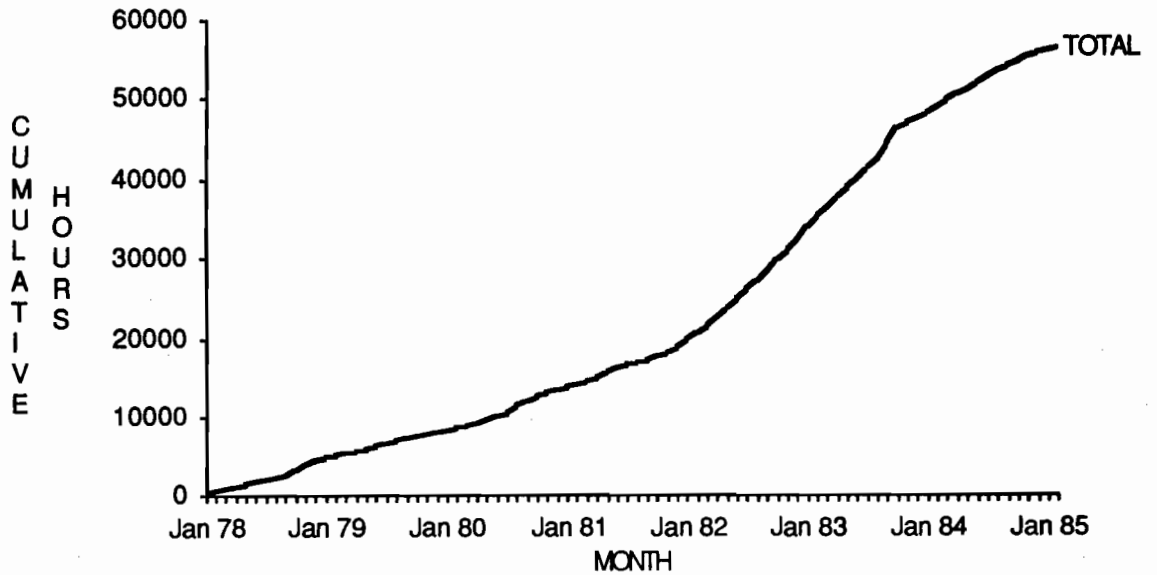


Figure 1. SCR activity.

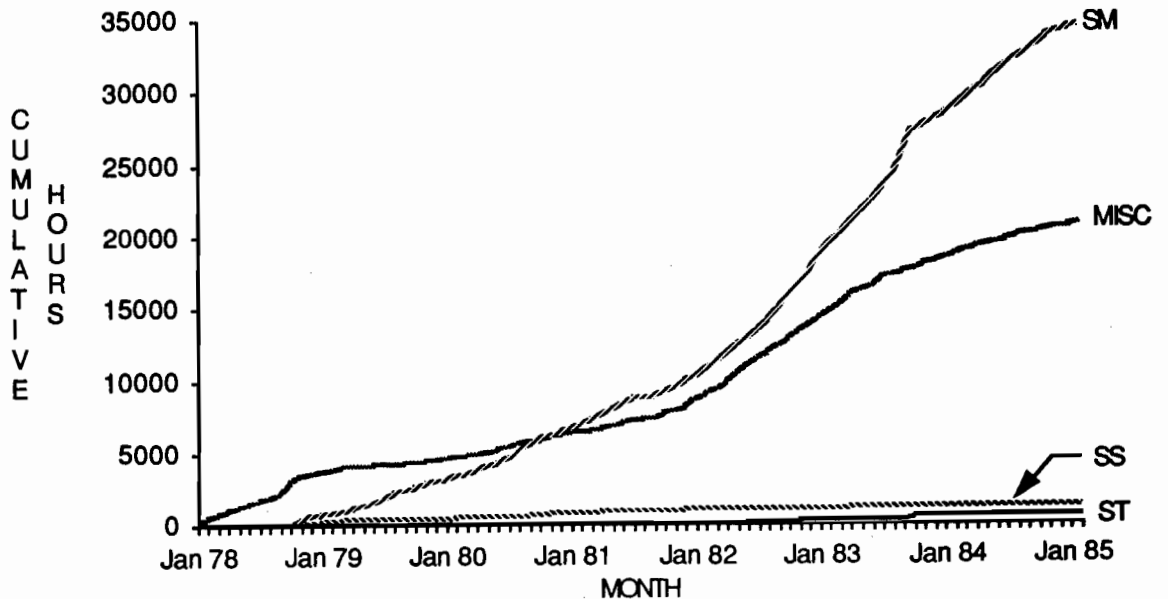
ware testing activity is reported as hours spent on general issues of computer-based testing and on testing of system subsets. *Miscellaneous* activity is reported as hours spent on activities not included in any of the above definitions.

3. OVERVIEW OF SCR PROJECT ACTIVITIES

From January 1978 to February 1985, over fifty-five thousand activities hours have been reported. Experiments have been performed to provide reasonable assurance that the reported hours accurately reflect project activity and are appropriately categorized [3]. The monthly accumulation of hours expended on all

activities is presented in Figure 1. The monthly accumulation of hours expended in the top level categories is presented in Figure 2. Software Structures (SS) effort is time spent defining and documenting hierarchical module structure in the A-7E module guide [2]. Software Modules (SM) effort is time devoted primarily to specifying and implementing modules. Software Testing (ST) effort is time spent on validation testing of subsets, and Miscellaneous (MISC) is time spent on all other

Figure 2. SCR area activities.



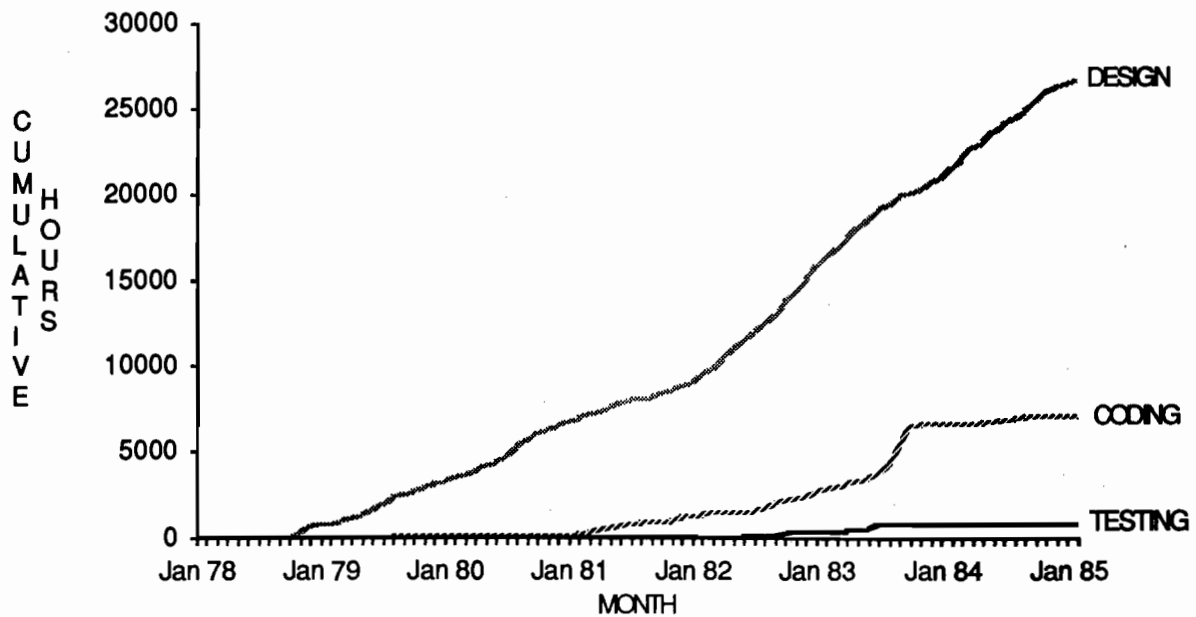


Figure 3. Software module activities.

activities such as travel and project control. Most SCR work so far has concentrated on software module development.

The monthly accumulation of hours expended in the Software Modules category on design, code (including pseudo-code), and test activities is presented in Figure 3. Over 75% of all reported software module activity is module design including redesign. This is consistent with the emphasis in the SCR methodology on extensive design with the expectation of significant reductions in coding, testing, and maintenance efforts [9].

There are three categories of first-level SCR modules: Hardware Hiding modules, Behavior Hiding modules, and Software Decision modules [2]. These, in turn, include ten categories of second-level modules, listed in Table 1. Each of the second-level modules is organized

Table 1. Abbreviations and Names of Second Level Software Modules

| Abbreviation | Name |
|--------------|------------------------|
| AT | Applications Data Type |
| DB | Data Banker |
| DI | Device Interface |
| EC | Extended Computer |
| FD | Function Driver |
| FLT | Filter |
| PM | Physical Model |
| SG | System Generation |
| SS | Shared Services |
| SU | System Utilities |

into several submodules (third-level modules) and some of these are further modularized. The EC module, with seven levels of submodules, has the deepest module structure.

Six of the second-level modules have accumulated more than 1000 hours of activity; these are EC, DI, FD, SS, AT, and PM. The six also have complete module interface specifications that are baselined or nearly baselined. In Figures 4 through 9, the monthly accumulation of hours expended on total activity and on design, code, and test activities are presented for each module.³ Only the EC and DI modules have appreciable amounts of coding and testing activities.

4. ANALYSES OF MODULE DESIGN DATA

The SCR project emphasizes careful design, which is reflected by the fact that design activity accounts for over 75% of all reported software module activity. One of the purposes of the data analyses was to identify parameters that characterize the design processes and offer predictive capabilities concerning them. Plots were constructed in order to characterize monthly hours expended on the subactivities of module design: design creating (DC), design discussing (DD), design peer reviewing (DR), design formal reviewing (DF), as well as total design (D). Unfortunately, characteristic patterns were not readily apparent.

³ Vertical lines in Figures 4 through 21 represent the dates on which baselined interface specifications for the respective modules were released. The absence of these lines on a specific plot indicates that no baseline documents have been released for that module.

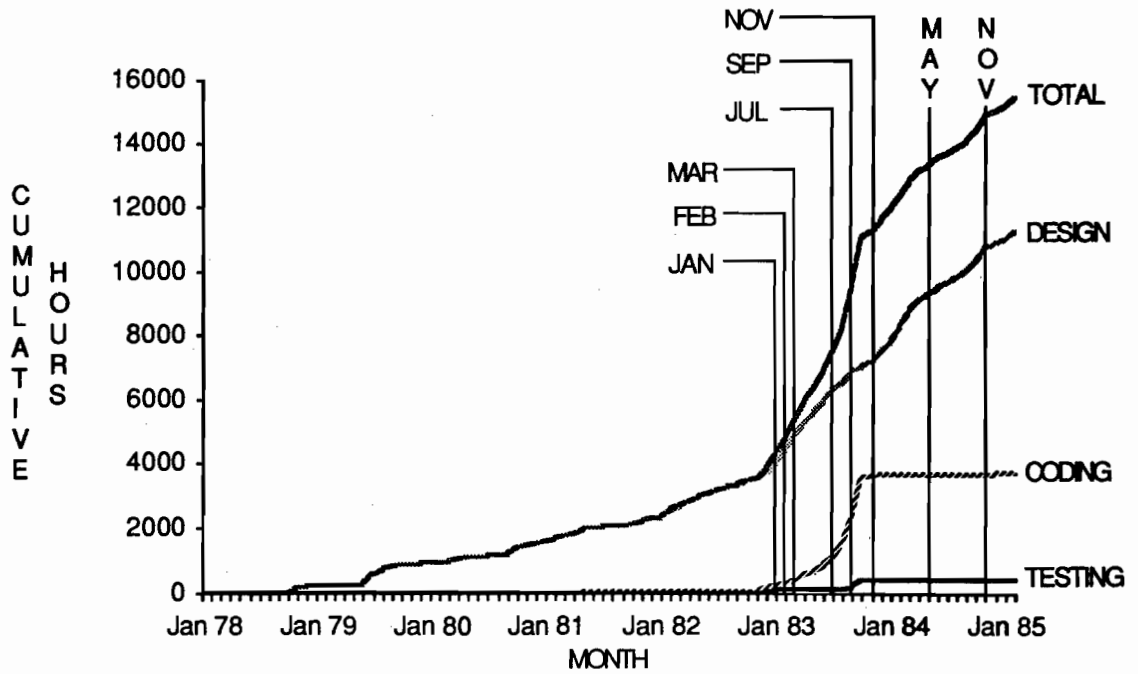


Figure 4. Extended computer activities.

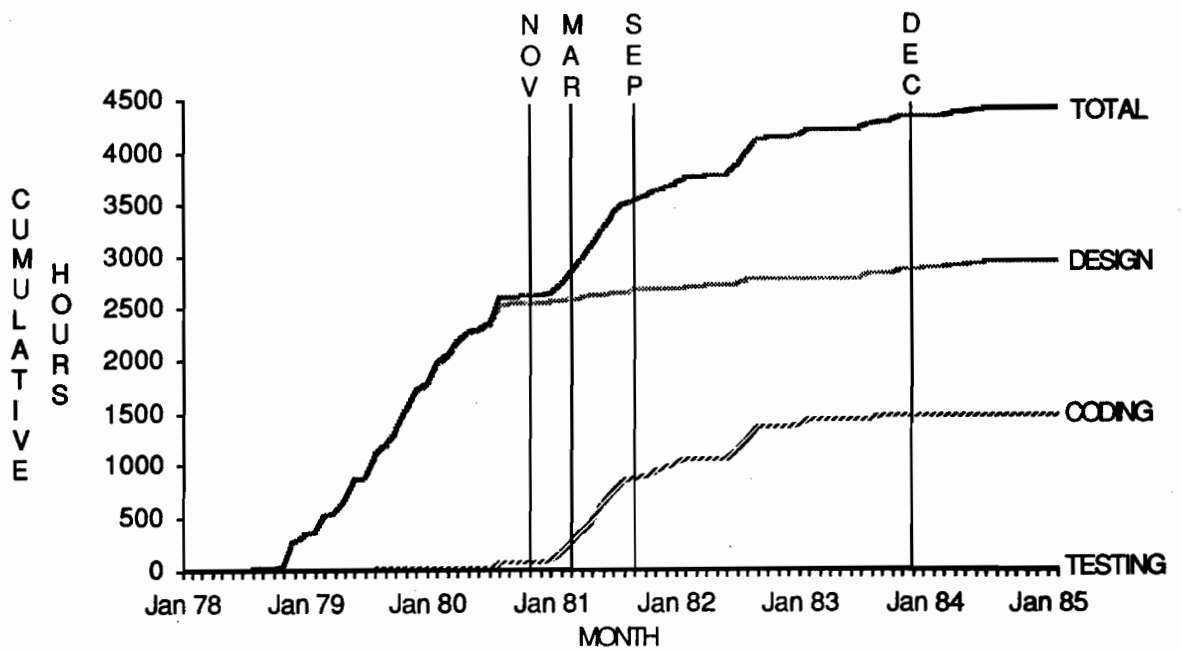


Figure 5. Device interface activities.

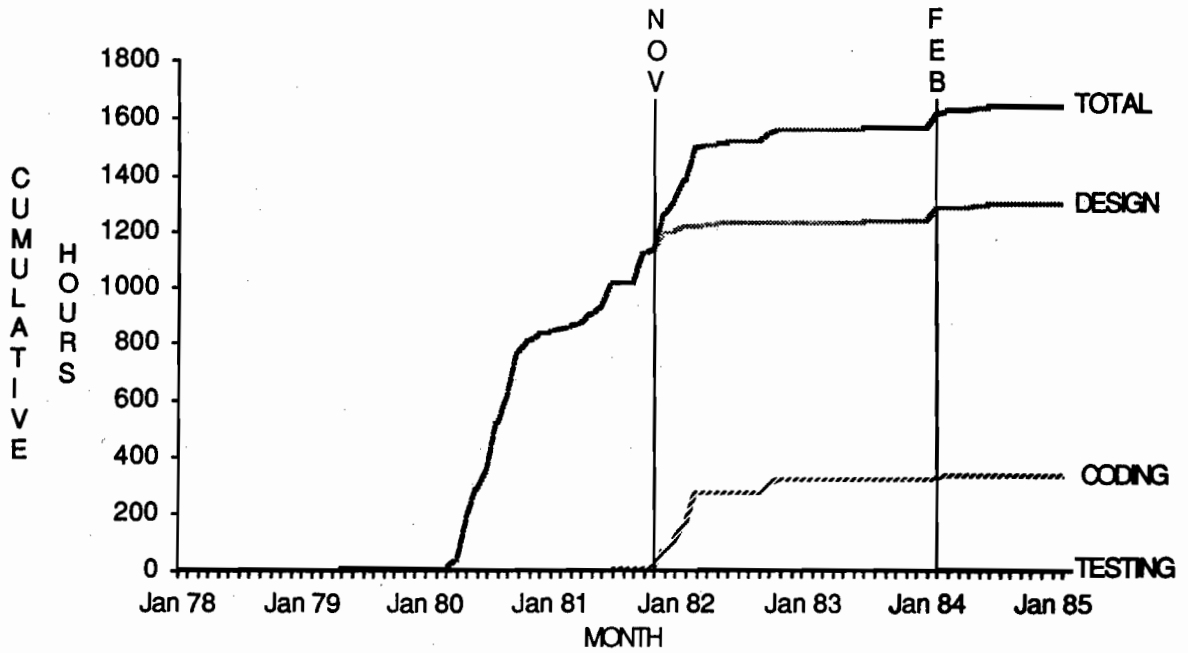


Figure 6. Function driver activities.

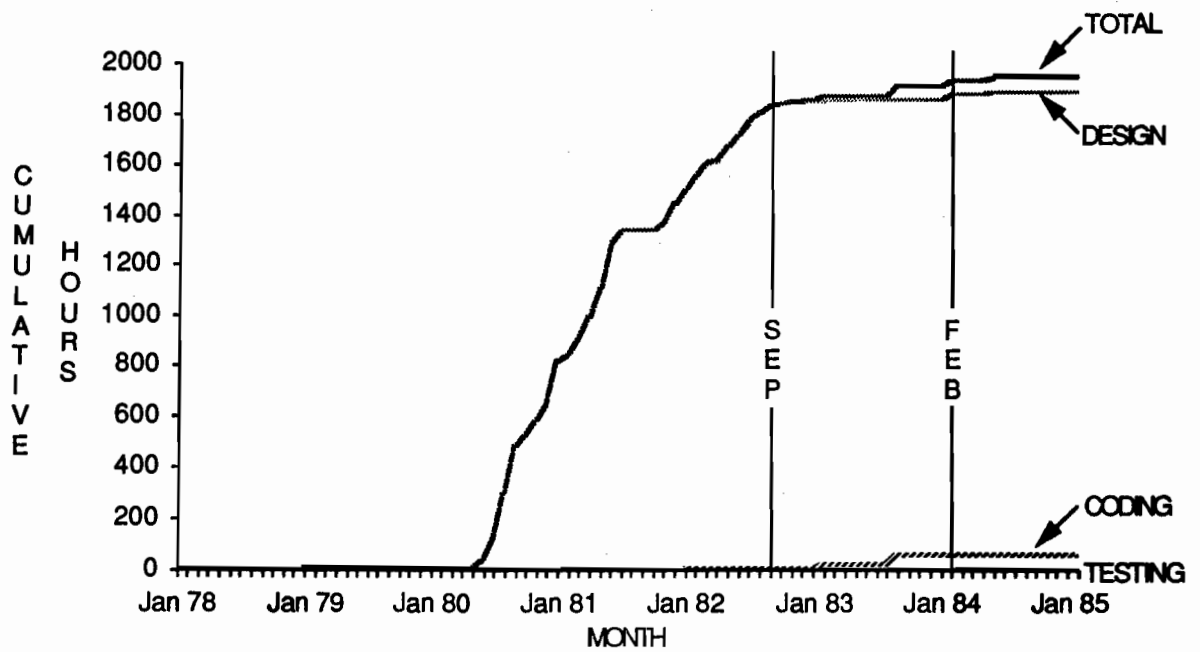


Figure 7. Shared services activities.

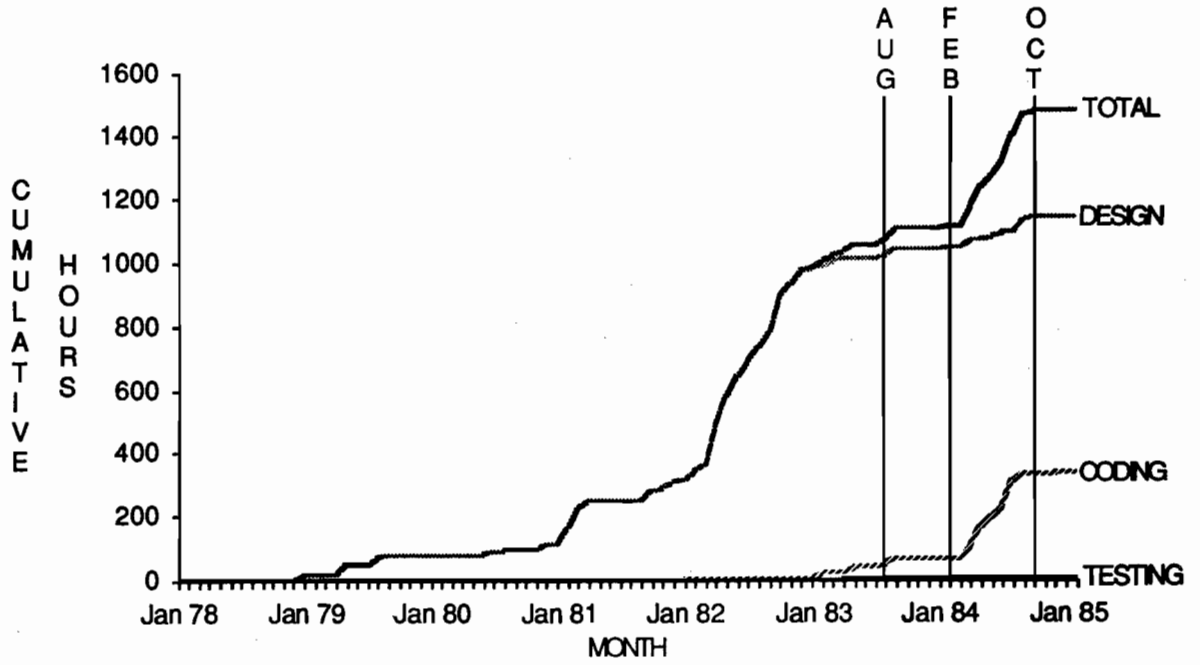


Figure 8. Applications data type activities.

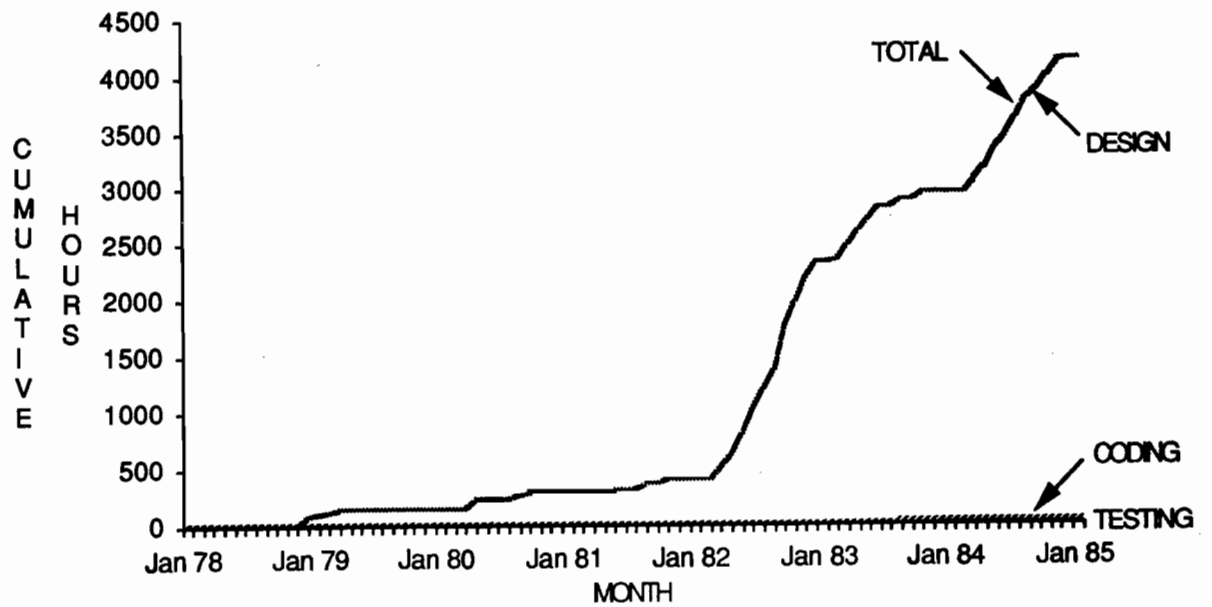


Figure 9. Physical model activities.

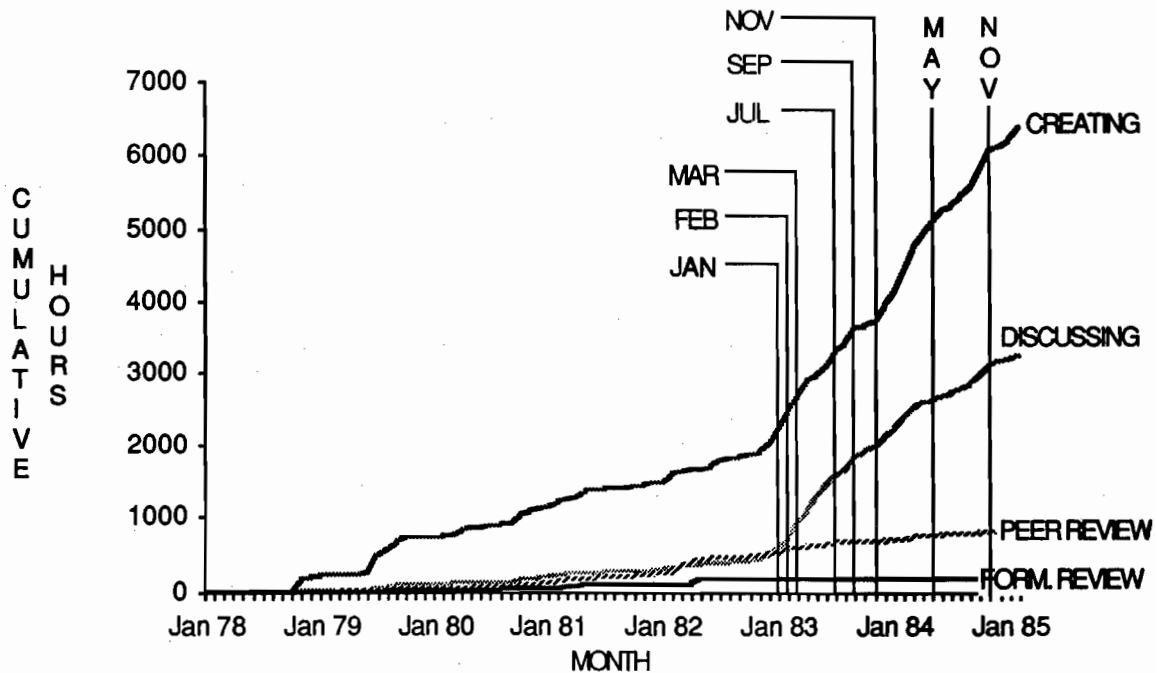


Figure 10. Extended computer design activities.

Subsequently, it was decided to examine the accumulation of hours expended on total design and design subactivities. This approach is considered appropriate because each data point reflects the history of design activities up to that point in time. Thus, the cumulative total design hours for a module is defined by:

$$\text{CumD}_n = \sum_{i=1}^n D_i$$

where D_i is the monthly total of all design activities on a module for month i . (Note that D_i includes design activity on all submodules of the module). Because data are available for all the months between January 1978 and February 1985, n has values from 1 to 86. Cumulative design creating hours for a module is defined by:

$$\text{CumDC}_n = \sum_{i=1}^n \text{DC}_i$$

where DC_i is the monthly design creating subactivity for a module (including all submodules) for month i . Again, n has values from 1 to 86. Similar definitions apply for CumDD_n and CumDR_n . The significant cumulative design activities for each module are shown in Figures 10 through 15.

An earlier study [3] highlighted the fact that ratios between activity categories provide valid and potentially useful metrics of SCR project activity. STE Project personnel intuitively suspected that ratios between activity categories could provide descriptive features of the SCR methodology that might be generally applicable to software design. Consequently, six ratio series between CumDC_n , CumDD_n , and CumDR_n were computed. For example, the ratio between cumulative design discussing and cumulative design creating is defined as:

$$(\text{CumDD}/\text{CumDC})_n = \frac{\text{CumDD}_n}{\text{CumDC}_n}$$

where n has values from 1 to 86. The other five, similarly defined, ratios are $(\text{CumDC}/\text{CumDD})_n$, $(\text{CumDC}/\text{CumDR})_n$, $(\text{CumDD}/\text{CumDR})_n$, $(\text{CumDR}/\text{CumDC})_n$, $(\text{CumDR}/\text{CumDD})_n$. These ratios were correlated with CumD_n over the 86 reporting months. Pearson correlation coefficients [6] are presented in Table 2. Next, for each module the ratio between monthly DC, DD, and DR were computed (e.g. DC_n/DD_n , DC_n/DR_n , and so on) and correlated with the total monthly D's and with the monthly CumD 's. These coefficients are presented in Tables 3 and 4.

V. RESULTS

An examination of the correlation coefficients reveals that the ratio $(\text{CumDD}/\text{CumDC})_n$ correlates consistently well with CumD_n , as shown in Table 2. This relationship

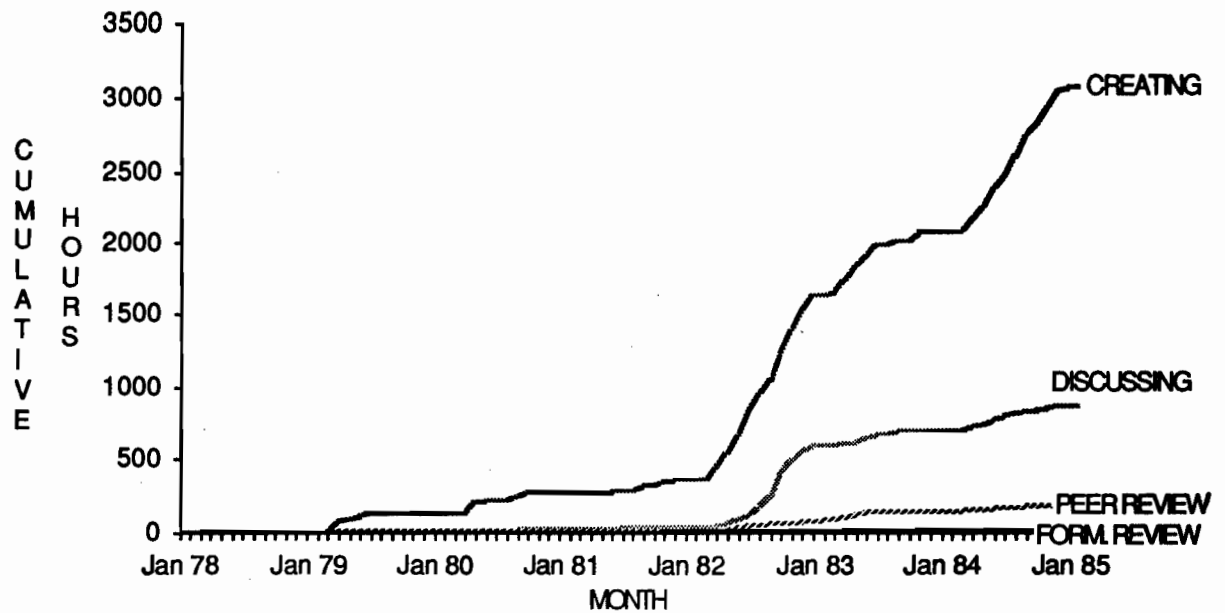


Figure 15. Physical model design activities.

Table 2. Pearson Correlation Coefficients between CumD and Cum. Ratios

| Module | CumDC/CumDD | CumDC/CumDR | CumDD/CumDC | CumDD/CumDR | CumDR/CumDC | CumDR/CumDD |
|--------|-------------|-------------|-------------|-------------|-------------|-------------|
| AT | -0.4034 | 0.1245* | 0.9774 | 0.9609 | 0.7483 | -0.2006* |
| DI | 0.0560* | -0.1998* | 0.6574 | 0.1002* | 0.8324 | 0.8124 |
| EC | -0.3785 | -0.3091 | 0.9492 | 0.6530 | 0.5436 | -0.0568* |
| FD | 0.7565 | -0.0897* | 0.9482 | -0.0252* | 0.1001* | 0.9575 |
| PM | -0.4090 | -0.4144 | 0.9052 | 0.1429* | 0.9235 | 0.3801 |
| SS | 0.9181 | 0.8665 | 0.5156 | 0.8408 | -0.3675 | 0.5437 |

* Not significant at the $p \geq .005$ level.

Table 3. Pearson Correlation Coefficients between D and Monthly Ratios

| Module | DC/DD | DC/DR | DD/DC | DD/DR | DR/DC | DR/DD |
|--------|----------|--------|---------|---------|---------|----------|
| AT | 0.3099 | 0.4031 | 0.3548 | 0.3048 | 0.3664 | 0.1572* |
| DI | 0.3759 | 0.4829 | 0.1040* | 0.2044* | 0.0227* | 0.2075* |
| EC | -0.0008* | 0.3972 | 0.3401 | 0.5396 | 0.0040* | -0.0998* |
| FD | 0.6470 | 0.5190 | 0.1305* | 0.4813 | 0.1042* | 0.3796 |
| PM | 0.3083 | 0.5845 | 0.3175 | 0.6581 | 0.0461* | 0.3491 |
| SS | 0.6509 | 0.6040 | 0.0461* | 0.4309 | 0.1248* | 0.2578 |

* Not significant at the $p \geq .005$ level.

Table 4. Pearson Correlation Coefficients between CumD and Monthly Ratios

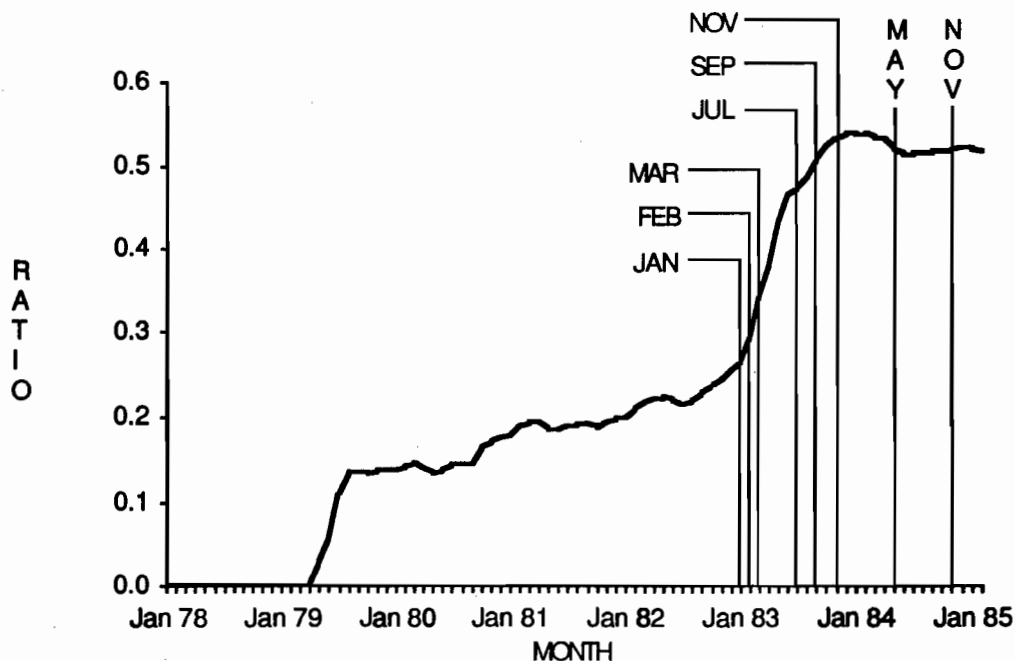
| Module | DC/DD | DC/DR | DD/DC | DD/DR | DR/DC | DR/DD |
|--------|----------|----------|---------|----------|----------|----------|
| AT | 0.0532* | 0.1667* | 0.1169* | 0.0843* | -0.0177* | -0.1287* |
| DI | -0.1693* | -0.1414* | 0.0344* | -0.0879* | 0.0683* | 0.0352* |
| EC | -0.0932* | 0.3933 | 0.3467 | 0.5236 | -0.0248* | -0.0886* |
| FD | -0.0034* | 0.0603* | 0.1409* | 0.0293* | 0.1032* | 0.1282* |
| PM | 0.4034 | 0.3568 | 0.1182* | 0.2205 | 0.170* | 0.2582 |
| SS | 0.0547* | -0.0447* | 0.1556* | -0.0531* | -0.0177* | 0.0815* |

* Not significant at the $p \geq .005$ level.

is evident from the plots of the ratios. In Figure 16, the monthly ratio for $(\text{CumDD}/\text{CumDC})_n$ is plotted for the EC module. Comparing this with Figure 10, it can be seen that design activity surges are characterized by prior or concomitant dramatic increases in this ratio. When this ratio remains constant, it is an indication that design activity has stabilized. Increases in this ratio seem to indicate design progress. Consequently, we refer to this as the progress indicator ratio (PIR).

Even though the EC module is extremely large and complex, the relationship seems strong. A large jump in design activity follows the large rise of the PIR. However, design activity for this module is not quite stabilized and the late downward trend in the ratio indicates increasing creating time relative to discussing time.

Figure 16. Progress indicator ratio for extended computer module.



The same patterns are also present for the DI module. As can be seen in Figures 12 and 17, the dramatic increase in design activity follows a dramatic increase in the progress indicator ratio. This same relationship holds for the FD, SS, AT and PM modules. See Figures 18 through 21.

Coefficients of determination (r^2), as defined in [6], between CumD_n and $(\text{CumDD}/\text{CumDC})_n$ are presented in Table 5 for each module. This ratio seems to explain a high percentage of the variation of CumD_n .

The analyses provide supporting evidence that the ratio $(\text{CumDD}/\text{CumDC})_n$ is an important measure of design activity progress in developing modules for complex software. When the PIR becomes constant, design activity appears to be at a very low level or even non-existent. When this ratio increases, design activity increases dramatically. The relationship between this ratio and CumD_n is the strongest of all the possible relationships examined in this study. In at least one

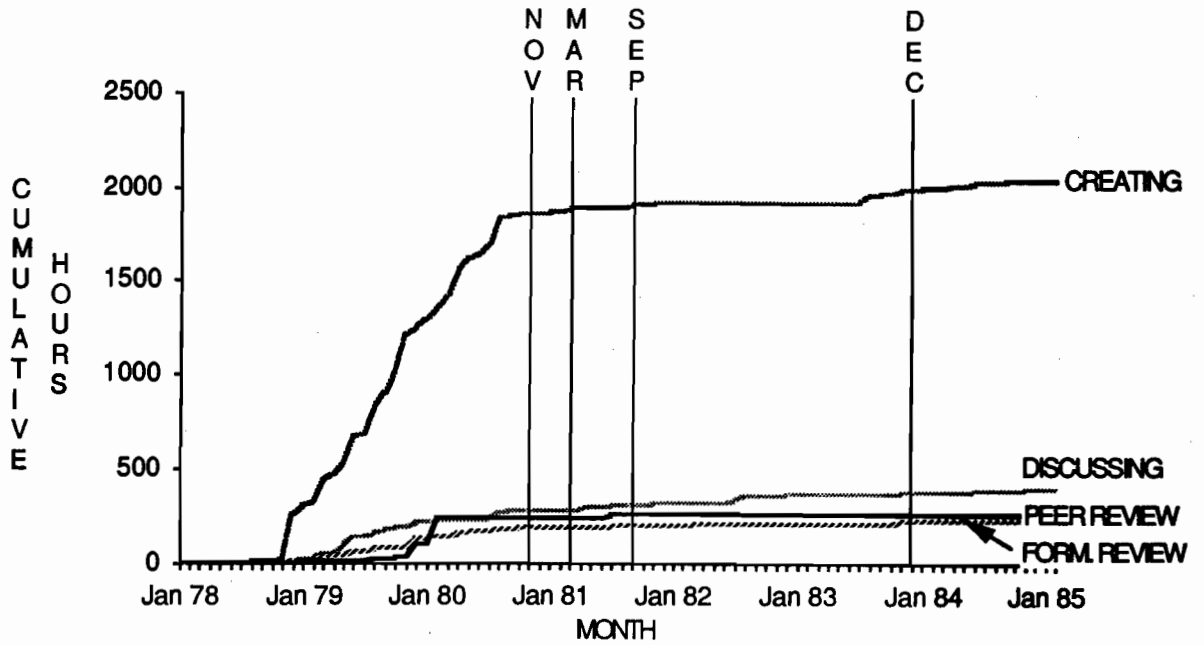


Figure 11. Device interface design activities.

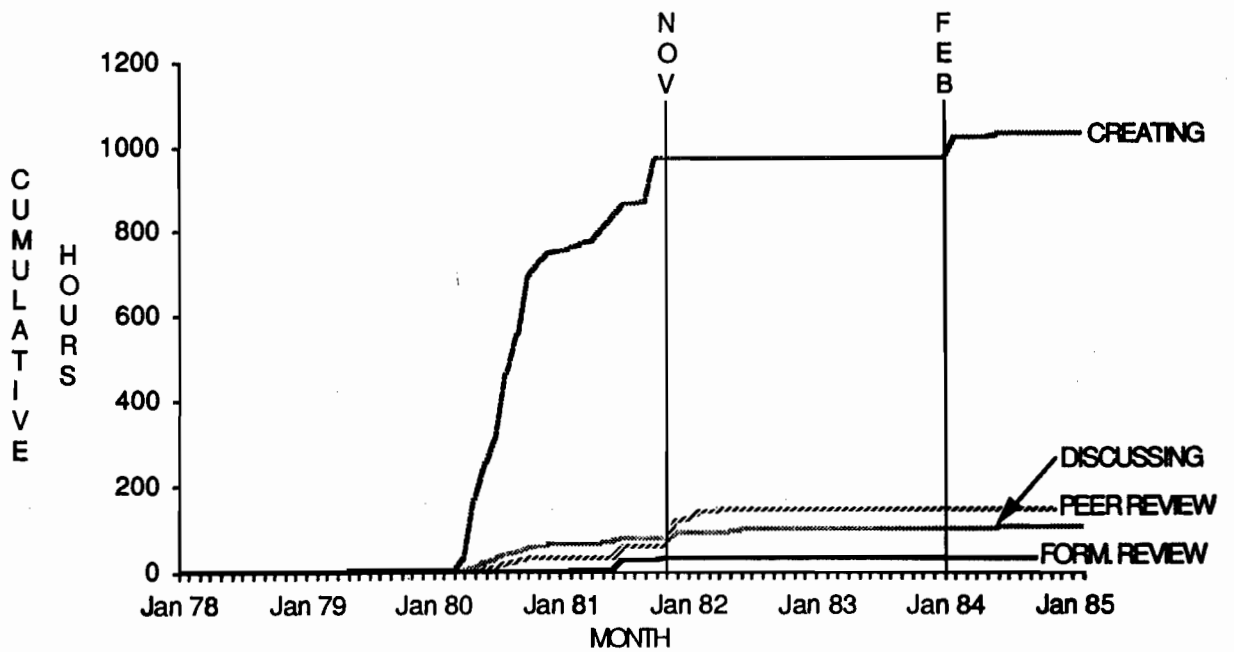


Figure 12. Function driver design activities.

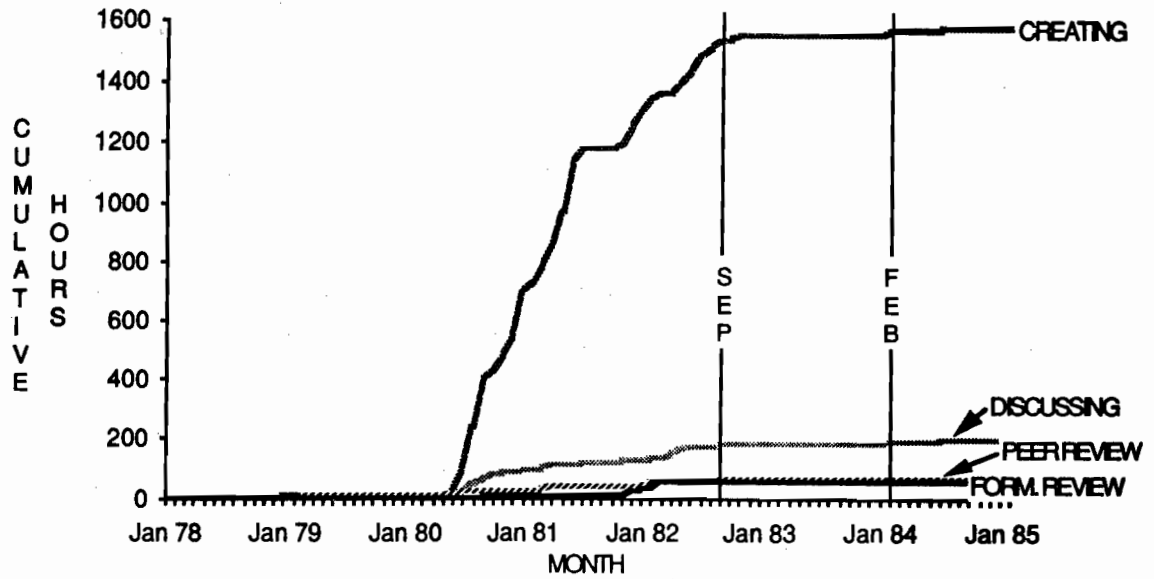


Figure 13. Shared services design activities.

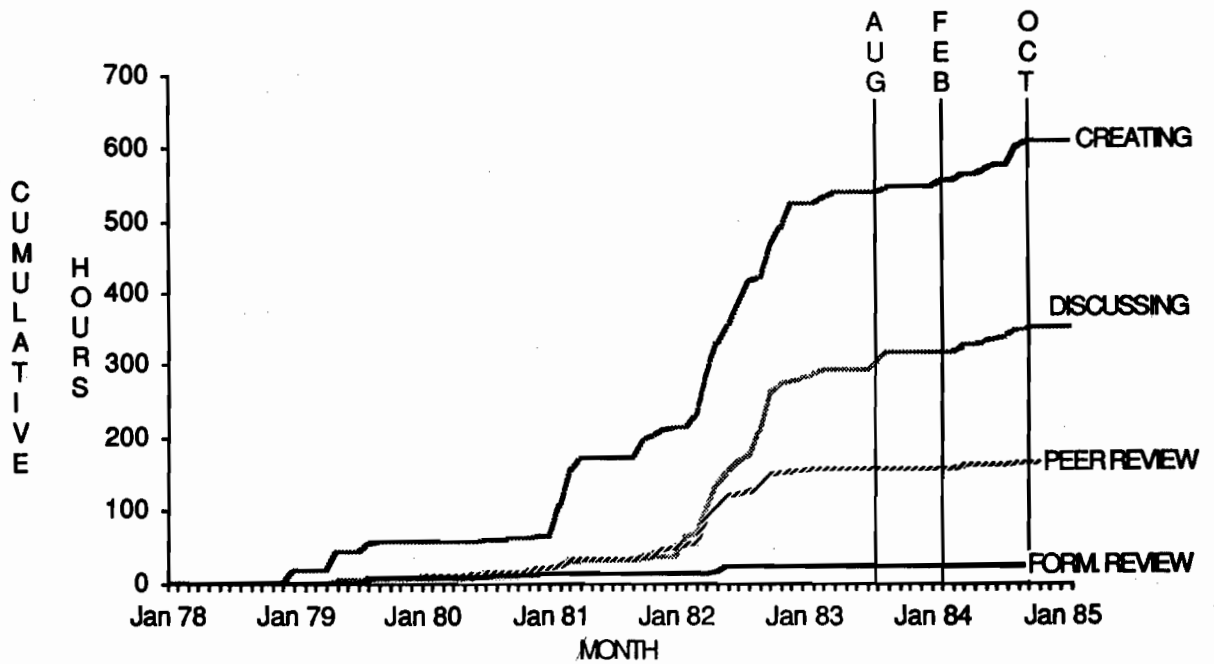


Figure 14. Applications data type design activities.

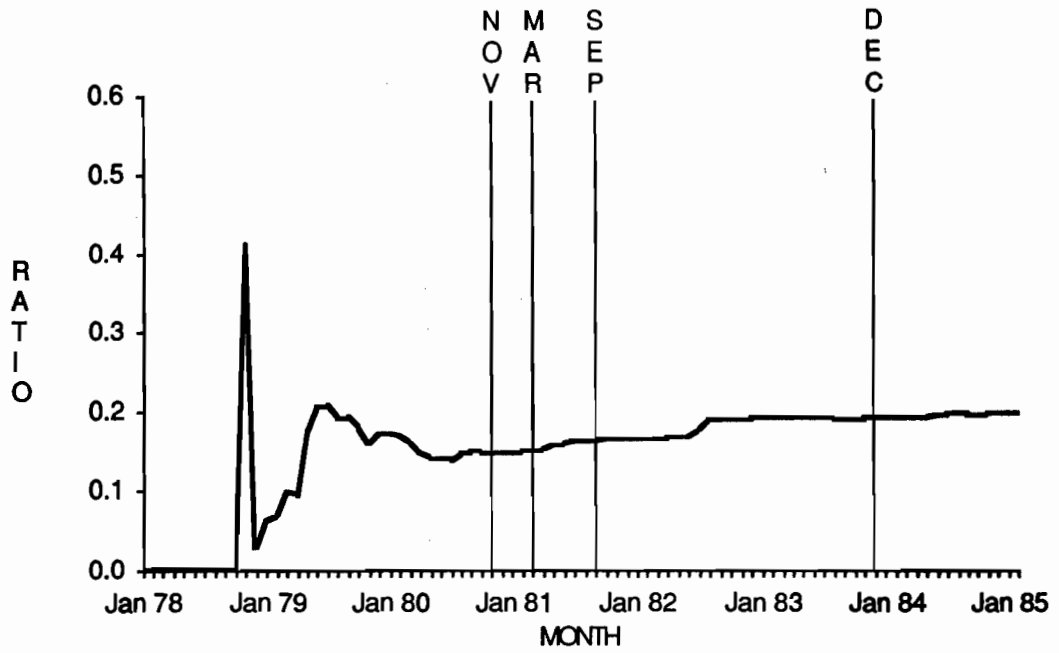


Figure 17. Progress indicator ratio for device interface module.

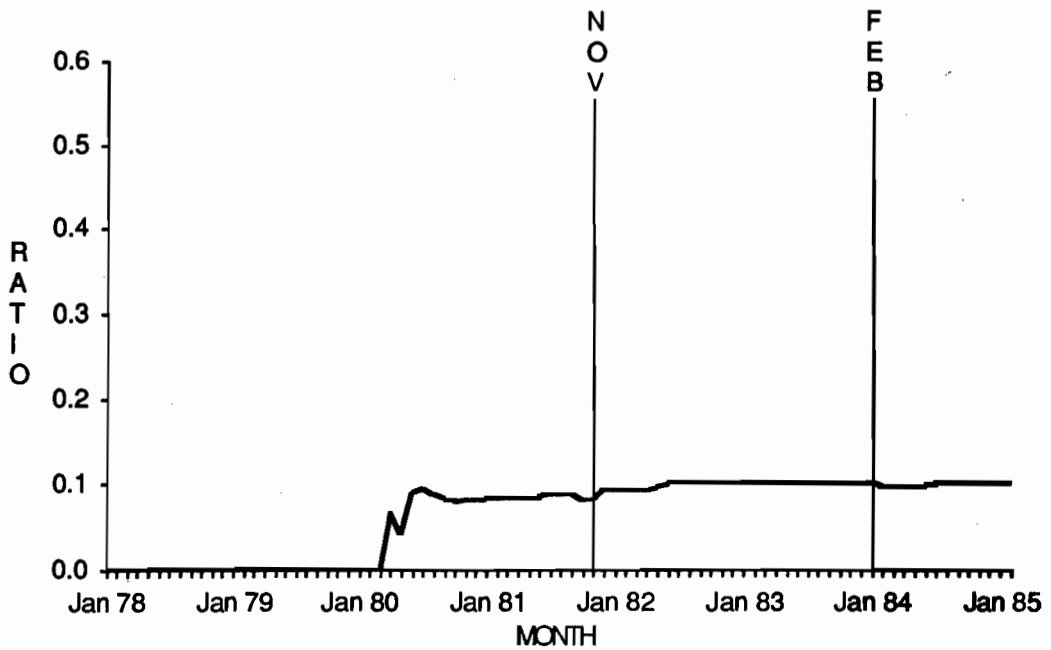


Figure 18. Progress indicator ratio for function driver module.

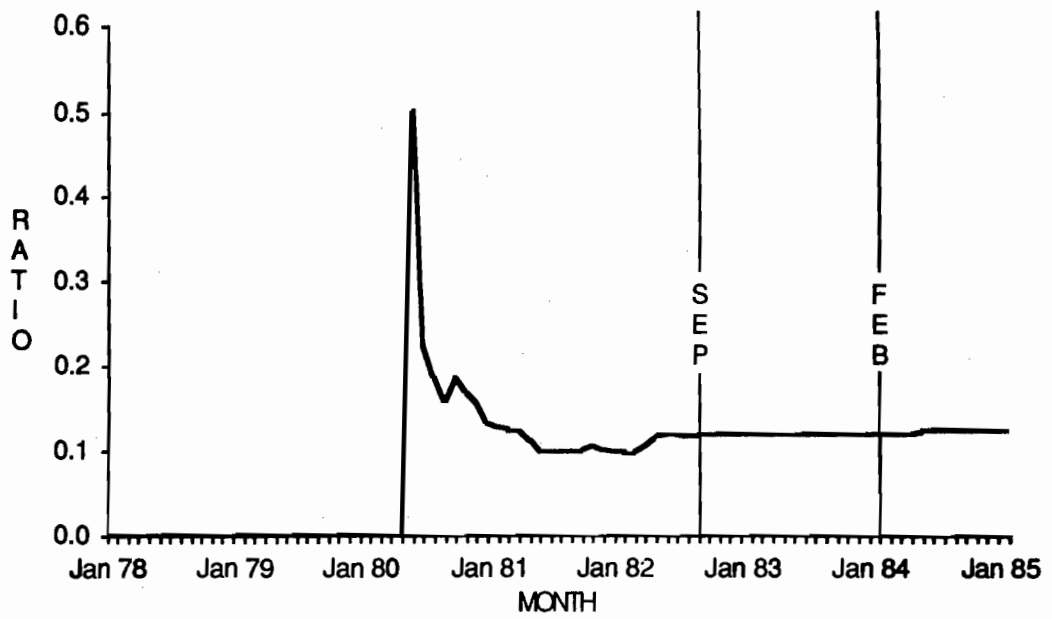


Figure 19. Progress indicator ratio for shared services module.

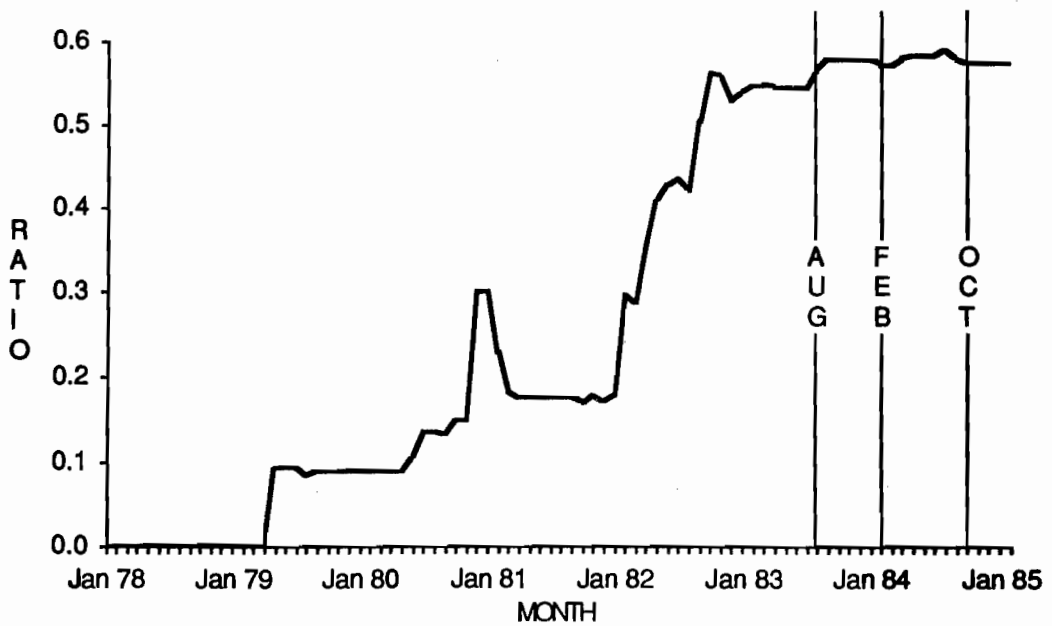


Figure 20. Progress indicator ratio for applications data type module.

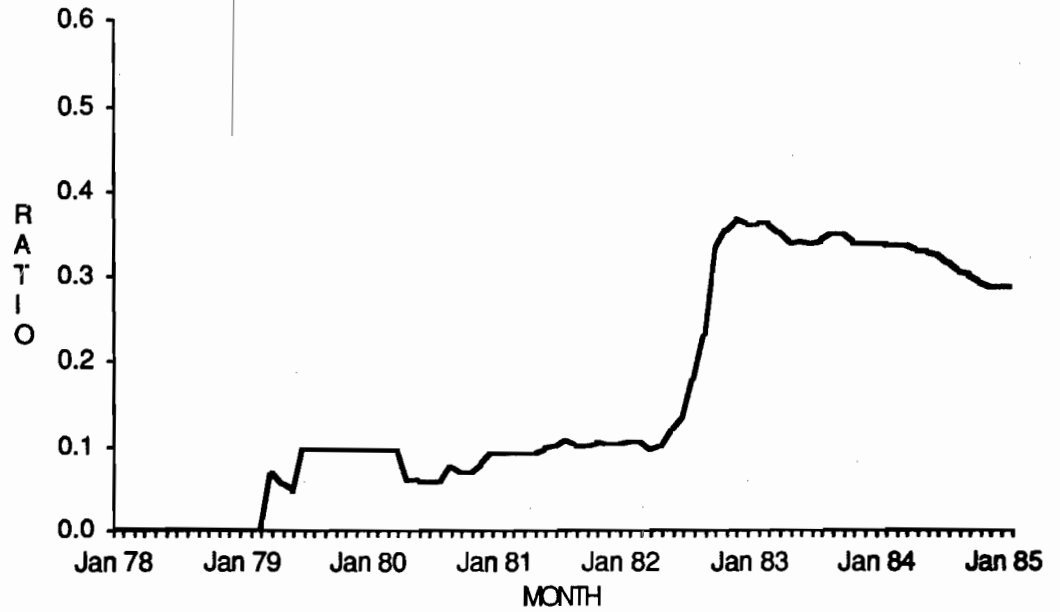


Figure 21. Progress indicator ratio for physical model module.

module, this ratio can explain over 95% of the variation in $CumD_n$. In the remaining modules, variations in $(CumDD/CumDC)_n$ can explain a surprisingly high degree of the variations in $CumD_n$.

6. CONCLUSIONS

A natural conclusion is that discussion between software designers is a critically important factor in the design of information hiding modules for complex software. When the release dates for specification baselines (e.g., [8]) are examined with the PIR, the PIR seems to be indicating the completeness of the baseline specifications. When a baseline appears before this ratio rises sharply or during a sharp rise, the baseline is probably far from complete. Abstract interface specifications would seem to become reasonably stable only after a sharp rise and settling of this ratio. Plotting this ratio over time may give the software manager a meaningful tool with which to track design progress. If the PIR has

not surged and stabilized, the design is probably not finished irrespective of personnel claims and published baseline documents.

In addition, the PIR has an attractive property not found in a monthly plot of $CumD_n$. The range of the y-axis is constant over time and over other modules and projects. Therefore, it is possible to compare design progress on one module or project to another using this ratio. The PIR does, however, have one possible negative property. Because it involves cumulative sums, the accumulation of earlier design hours can dampen the impact of later variations in design activity. The PIR for the EC module indicates, however, that this possible flaw may be more theoretical than practical.

There is no claim that the PIR is a measure of design completeness. There are clearly other reasons why design activity on a specific software module may have stabilized. Personnel may have shifted work to another module; they may have been on vacation, and so on. However, the PIR ratio does seem to provide an indication when work on a piece of software is definitely not finished. If design completion is claimed prior to a rise and settling in this ratio, there is probably more work that needs to be done on that module.

It is necessary that this analysis be replicated on other large scale software development projects to determine whether the PIR behaves similarly in other software development environments using different design methodologies. It is intuitively appealing that discussion between project members necessarily enhances the

Table 5. Coefficients of Determination (r^2) between $CumD$ and $CumDD/CumDC$

| Module | r^2 |
|--------|--------|
| AT | 0.9552 |
| DI | 0.4322 |
| EC | 0.9010 |
| FD | 0.8992 |
| PM | 0.8194 |
| SS | 0.2658 |

All are significant at the $p \geq .005$ level.

design of software modules. It would also be useful to quantify the relative surges in the PIR. That is, there is practical importance in knowing that a given percentage increase in the PIR is customarily followed by a predictable percentage increase in design activity. This, too, requires replicating these analyses in several different software design environments. Unfortunately, these data are difficult to collect and it is, perhaps, even more difficult to validate their accuracy.

Finally, it is logical to examine coding data for these relationships. It seems reasonable to accept the importance of discussion in the design process. Its importance in the coding and testing processes is not as clear. These data do exist in the SCR data base and plans are underway to examine them.

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