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HfO_2-insulated gate N-polar GaN HEMTs with high breakdown voltage

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In this paper, we present the first demonstration of a HfO_2-insulated gate N-polar GaN inverted high-electron-mobility transistor (iHEMT). HfO_2-insulated gate devices showed an order of magnitude improvement in reverse-bias gate leakage current as compared to reference Schottky devices. With the reduced gate leakage current, the insulated gate iHEMTs were able to simultaneously demonstrate breakdown voltages in excess of 130 V and maximum current density of 0.87 A/mm. Pulsed *I–V* gate-lag measurements were performed to investigate the drain current transient behavior of these devices.

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1 Introduction The vast majority of GaN high-electron-mobility transistor (HEMT) research to date has focused on Ga-polar (0001) wurtzite GaN crystalline material. N-polar $(000\bar{1})$ GaN has received little attention until only a few years ago, when Rajan et al. demonstrated a series of N-polar GaN/AlGaN/GaN HEMTs [1, 2]. Since that time, research in the area of N-polar GaN has gained momentum and is starting to demonstrate the potential of this material system. One advantage that the N-polar inverted HEMT (iHEMT) has over the conventional Ga-polar HEMT is that its ohmic contacts can be formed without alloying through a wide bandgap material such as AlGaN, InAlN, or AlN. Dasgupta et al. [3] have been able to achieve an extremely low ohmic contact resistance of 27 Ω μm to a N-polar GaN iHEMT channel through the use of non-alloyed, molecular-beam epitaxy (MBE) regrown graded InGaN to InN contacts. A second advantage of the iHEMT is that it contains a natural back-barrier, whose structure and composition can be controlled independently of the gate-to-channel distance. Wong et al. [4] have shown that dual-AlN back-barrier structures with sub-barrier Si delta doping can be used to achieve 71% power-added efficiency (PAE) and over 6 W/mm RF output power density at 4 GHz. These reported attributes of N-polar GaN devices suggest that this technology may be aptly suited for millimeter-wavelength frequency applications such as RF power amplifiers or ultrahigh-speed logic.

In this paper, we present the first demonstration of an iHEMT that utilizes an atomic-layer deposited (ALD) HfO_2 gate dielectric. HfO_2, as a gate insulator, potentially offers a greater opportunity for heterostructure vertical scaling as compared to previously reported SiN gate insulators [4–6] due to its higher dielectric constant [7]. With state-of-the-art iHEMT GaN channel layer thicknesses decreasing to 10 nm [8] and below, we anticipate that the use of high-κ dielectrics will help to suppress excess gate leakage current while maintaining high intrinsic gate capacitance. As a result, the potential benefits for ultra-short gate length iHEMT devices could include reduced f_T–L_G product roll-off [9, 10] and the ability to sustain higher operating voltages. The electrical characterization results reported in this paper indicate that off-state drain voltages of greater than 130 V can be achieved through the use of a 5 nm HfO_2 gate insulator and a relatively thick 42% Al mole fraction AlGaN back-barrier (Fig. 1).

2 Experimental The N-polar heterostructure used in this study was grown on the C-face of a 4H SiC wafer by plasma-assisted MBE in a Vacuum Generators V80H MBE system, which has been described previously [11]. The surface pretreatment before growth consisted of an organic solvent clean, 25 min UV/ozone oxidation treatment at room temperature, followed by an HF dip and deionized (DI) water rinse to remove residual surface oxide. The 50 nm thick AlN nucleation layer growth was followed by a two-step [14]

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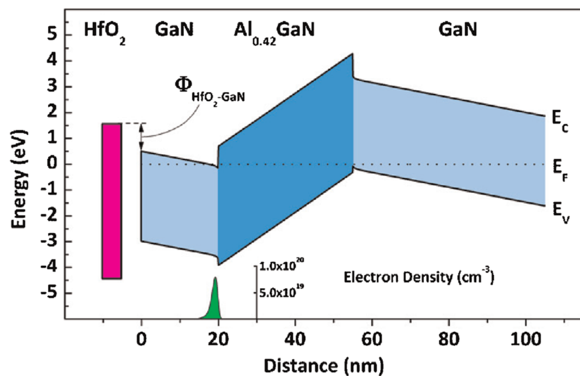

Figure 1 (online color at: www.pss-a.com) N-polar inverted HEMT band diagram [12] showing the theoretical HfO_2–GaN conduction band offset [13].

0.6 μm GaN buffer. No intentional Si-doping was used in the active device heterostructure, which consisted of a 35 nm $Al_{0.42}$GaN barrier layer capped with a 20 nm GaN channel layer. The as-grown sheet resistance of this sample, as determined by contactless sheet resistance measurement, was 393 Ω/□. No signs of lattice relaxation, such as sheet resistance degradation or visual cracking were observed after growth or device processing.

Device fabrication began with ohmic contact definition and metallization. An unoptimized Ti/Al/Ni/Au ohmic metal stack was deposited by e-beam evaporation after a low-power BCl_3/Cl_2/Ar dry etch, lifted off using heated *n*-methyl-pyrrolidone-based 1165 resist stripper, and annealed at 850 °C for 30 s. Circular transfer length measurements showed that contact resistance was 3 Ω mm. Device source–drain and gate–drain spacing were 5 and 2 μm, respectively. Following ohmic contact metallization, an inductively-coupled plasma (ICP) BCl_3/Cl_2/Ar dry etch was used to produce mesas for isolation. Interdevice isolation current was measured to be less than 1 nA at 100 V across a circular isolation test pattern with a 16 μm mesa-to-mesa gap and center metal contact diameter of 100 μm. Room temperature Hall measurements revealed that the electron channel sheet resistance was 418 Ω/□, Hall mobility was 1070 cm^2/V s, and sheet carrier density was 1.4×10^{13} cm^{-2}. Prior to gate insulator deposition, a portion of the wafer was patterned with Ni/Au (20/300 nm) Schottky gates to serve as reference devices.

To fabricate MIS gates, the HEMT surface was first treated with buffered HF for 30 s and then rinsed in DI water. After 10 min of thermal equilibriation at 250 °C, a thin 5 nm layer of HfO_2 was blanket deposited by ALD in a hot-wall flow tube type reactor [15]. During the deposition process, the gaseous precursors tetrakis ethyl methyl amino hafnium (TEMAHf) and DI water were alternatively pulsed using 1–1.5 s pulses for TEMAHf, 0.5 s pulses for H_2O, and 30 s purge times. A 14 sccm constant flow of ultrahigh purity N_2 gas was used to maintain a pressure of 200 mTorr during deposition. Forty-five cycles were used to achieve the desired thickness, based on a ~1 Å/cycle growth rate determined by spectroscopic ellipsometry measurements of the HfO_2 film on Si. After deposition, Ni/Au (20/300 nm) gate contacts were patterned using standard photolithographic techniques. Scanning electron microscope images taken after electrical testing showed that the gate length of the devices used in this study was 1.8 μm. The gate width was 2 × 25 μm.

3 Results and discussion

To evaluate the performance of the devices in this study dc *I–V* and pulsed *I–V* gate-lag measurements were taken. Figure 2 shows a split-wafer comparison of gate *I–V* for a Schottky gate iHEMT and a HfO_2-insulated gate device. During the measurement, the source and drain terminals were grounded. Under significant negative gate bias, the insulated gate devices showed a factor of 10X reduction in gate leakage current as compared to the Schottky devices.

The observed insulated gate *I–V*, however, was asymmetric and reached higher current values under forward bias. This Schottky-like behavior could possibly be the result of incomplete coalescence of the HfO_2 film underneath the gate metal, or may be indicative of electron thermionic and/or tunneling transport across the HfO_2 barrier.

Figure 3 illustrates the drain *I–V* behavior for an insulated gate device. The maximum drain current, as determined by the drain transfer curve inset of Fig. 3, reached 0.87 A/mm at a gate–source voltage of 4 V with the drain–source voltage equal to 10 V. Extrinsic transconductance was limited to 160 mS/mm, but if voltage drops across source contact and access resistances were taken into consideration, intrinsic transconductance was extracted to be 368 mS/mm. The Schottky reference device suffered from excessive gate leakage current, which allowed for partial modulation of the 2DEG channel but prohibited pinch-off from being achieved.

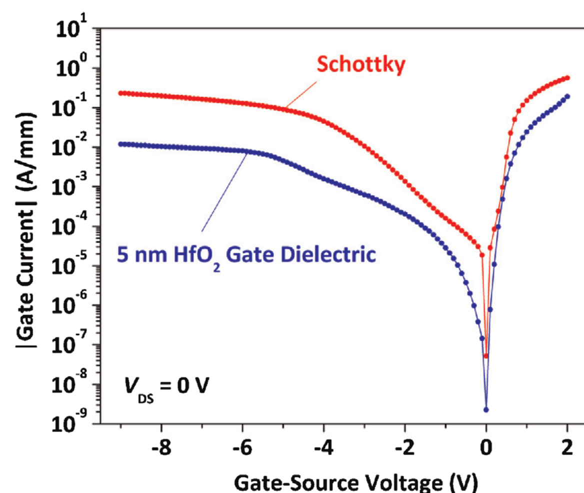

Figure 2 (online color at: www.pss-a.com) Split-wafer comparison of gate *I–V* for GaN iHEMTs with and without a 5 nm HfO_2 gate insulator.

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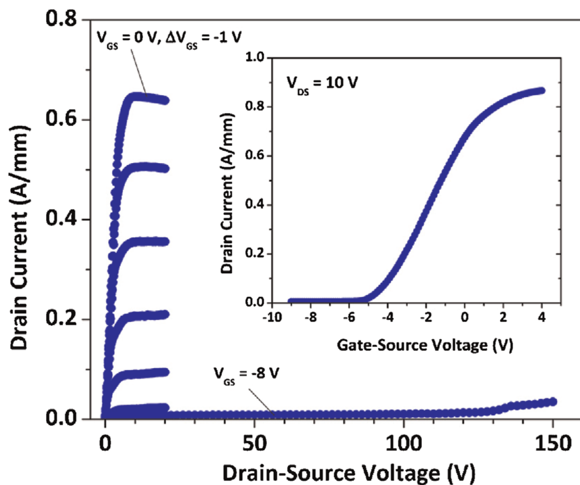

Figure 3 (online color at: www.pss-a.com) Drain *I–V* for a HfO_2-insulated gate iHEMT. Inset shows drain current versus gate–source voltage for $V_{DS} = 10$ V.

Also shown in Fig. 3 is the off-state breakdown character of the HfO_2-insulated gate device, which was measured with the gate biased at −8 V. Soft breakdown behavior occurred at approximately 130 V when the drain current started to rise with increasing drain voltage. This increase was also accompanied by a rise in gate leakage current, suggesting that drain-to-gate current is likely responsible for the observed breakdown. The demonstration of both high off-state drain voltage tolerance and high maximum current density in this sample suggests that high power operation may be achievable with this type of insulated-gate device design.

Pulsed *I–V* gate-lag measurements shown in Fig. 4 suggest that trapping phenomena are likely present in the HfO_2-insulated gate iHEMT device. The drain current transient behavior consisted of two parts; first, there was a

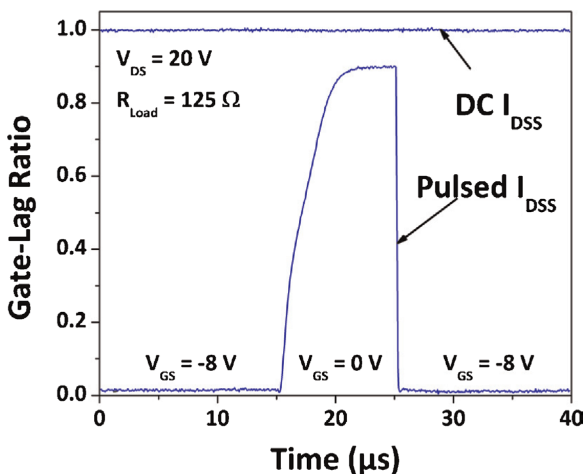

Figure 4 (online color at: www.pss-a.com) Pulsed *I–V* gate-lag measurement of a HfO_2-insulated gate iHEMT.

drain current rise-time of approximately 7 μs, followed by a leveling off to a gate-lag ratio of 0.9. This behavior is qualitatively different than what is typically observed in unpassivated Ga-polar HEMTs, whose drain current transients quickly rise and level off to values between 0.1 and 0.7 in less than 0.5 μs [16, 17]. The mechanism responsible for the observed drain current transient in Fig. 4 may be related to a donor-like trap state, previously suggested by Rajan et al. [2], located near the lower AlGaN/GaN interface.

4 Conclusions This paper discusses dc *I–V* and pulsed *I–V* gate-lag electrical characterization results of HfO_2-insulated gate iHEMTs. With an order of magnitude reduction in gate leakage current as compared to Schottky reference devices, the insulated gate iHEMTs were able to simultaneously demonstrate high maximum current density and high breakdown voltage. When combined with the other inherent benefits of the iHEMT, we expect that high-κ gate dielectrics will enable new high frequency applications for GaN technology.

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