High Electron Velocity Submicrometer AlN/GaN MOS-HEMTs on Freestanding GaN Substrates

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***Abstract*—AlN/GaN heterostructures with 1700-cm^2/V · s Hall mobility have been grown by molecular beam epitaxy on freestanding GaN substrates. Submicrometer gate-length (L_G) metal–oxide–semiconductor (MOS) high-electron-mobility transistors (HEMTs) fabricated from this material show excellent dc and RF performance. $L_G = 100$ nm devices exhibited a drain current density of 1.5 A/mm, current gain cutoff frequency f_T of 165 GHz, a maximum frequency of oscillation $f_{\max}$ of 171 GHz, and intrinsic average electron velocity v_e of 1.5×10^7 cm/s. The 40-GHz load-pull measurements of $L_G = 140$ nm devices showed 1-W/mm output power, with a 4.6-dB gain and 17% power-added efficiency. GaN substrates provide a way of achieving high mobility, high v_e, and high RF performance in AlN/GaN transistors.**

***Index Terms*—Atomic layer deposition, AlN, GaN, high-electron-mobility transistors (HEMTs), HfO_2, hydride vapor phase epitaxy (HVPE).**

I. Introduction

RECENT research to increase the frequency performance of GaN high-electron-mobility transistors (HEMTs) has focused on aggressively scaling the device geometry. As GaN HEMT gate lengths L_G are reduced below 0.25 μm, the demands of electrostatic control have led to the use of novel ultrathin barriers with higher Al mole fractions than conventional AlGaN alloys. For Ga-polar heterostructures, AlN is the thinnest pseudomorphic barrier material available that can induce (via polarization and conduction band discontinuity) a 2-D electron gas (2DEG) density suitable for transistor use in GaN [1]. Early reports of RF devices based on the AlN/GaN heterostructure showed the potential of scaling the barrier thickness by demonstrating current gain cutoff frequency f_T values in the 50- to 110-GHz range [2], [3]. More recently, dramatic reduction in source–drain spacing L_{SD} down to 100 nm, selective regrowth of n$^+$ GaN source and drain regions by molecular beam epitaxy (MBE), and AlGaN back barriers have been used to demonstrate the highest combination of $f_T = 310$ GHz and the maximum frequency of oscillation $f_{\max}$ of 364 GHz for depletion-mode GaN HEMTs to date [4].

While device engineering can be used to minimize certain electron delay components such as parasitic and channel charging, the primary constituents of total electron delay $(2\pi f_T)^{-1}$ are typically the drain delay and intrinsic gate transit times, which are inversely proportional to the average electron velocity v_e in their respective regions [4], [5]. The goal of this study was to determine whether higher v_e can be achieved with the use of hydride vapor phase epitaxy (HVPE)-grown freestanding GaN as a substrate for AlN/GaN HEMT device epitaxy. Since epitaxial layers can be grown with a low dislocation density ($< 10^7$ cm^{-2}) on HVPE GaN [6], this substrate offers a lattice- and thermal-expansion-matched platform for heterostructure growth that has potential advantages over previously examined substrates such as Si [7], sapphire [1]–[3], [8], [9], and SiC [4], [5], [9]–[12]. To evaluate the dc and RF electrical performance of this material, we fabricated and tested submicrometer T-gate AlN/GaN MOS-HEMT devices, as schematically shown in Fig. 1.

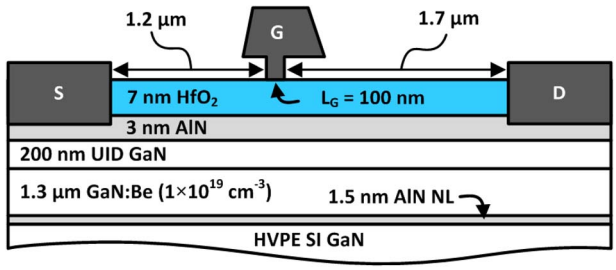

Fig. 1. Cross-sectional schematic of an $L_G = 100$ nm AlN/GaN MOS-HEMT.

II. Experiment

The HEMT structure was grown by RF-plasma-assisted MBE on a 1 cm × 1 cm freestanding HVPE-grown GaN semi-insulating substrate at 650 °C. Following a 60-s surface nitridation of the GaN substrate, growth began with a 1.5-nm-thick AlN nucleation layer [13]. A 1.3-μm-thick GaN layer was then grown with beryllium doping used to suppress buffer leakage current [14]. Finally, a 200-nm-thick unintentionally doped (UID) GaN buffer layer was grown and capped with a

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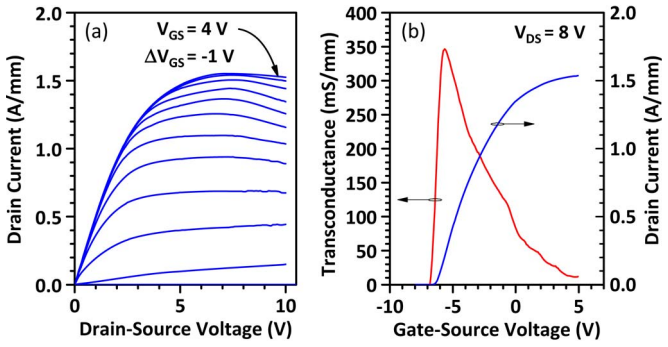


Fig. 2. (a) Drain and (b) transfer curves for an $L_G = 100$ nm AlN/GaN device.

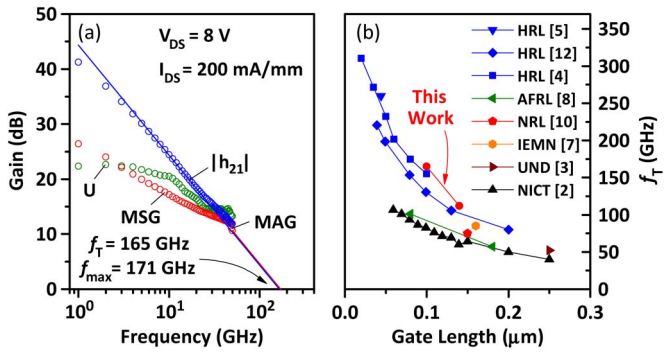
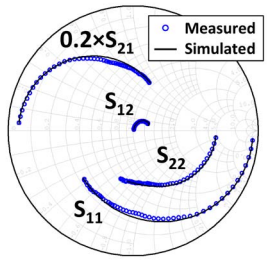


Fig. 3. (a) Pad deembedded small-signal characteristics of an AlN/GaN device with $L_G = 100$ nm. (b) f_T results from this study ($L_G = 100$ and 140 nm) *compared with* other previously reported AlN/GaN HEMT small-signal f_T.

Equivalent Circuit Model Parameters

L_G = 100 nm W_G = 2 × 75 μm	Bias Conditions V_{DS}=8V/V_{GS}= -5.25 V
g_m (mS)	75.2
g_d (mS)	5.1
C_{gs} (fF)	49.3
C_{gd} (fF)	14.0
R_i (Ω)	1
R_g (Ω)	5
R_s (Ω)	4
R_d (Ω)	4



Calculated Values

Delay Component	Value (ps)
Parasitic charging	0.11
Channel charging	0.03
Drain delay	0.19
Intrinsic gate transit	0.66
Total electron delay	0.99

Figures of Merit	
$f_{T,model}$ (GHz)	161
$f_{T,measured}$ (GHz)	165
$f_{max,model}$ (GHz)	176
$f_{max,measured}$ (GHz)	171
Intrinsic v_e (cm/s)	1.53×10^7

Fig. 4. Equivalent circuit modeling results and extracted parameters of the $L_G = 100$ nm AlN/GaN device in Fig. 3(a).

3-nm AlN barrier layer. The GaN layers were grown in a metal-rich regime at a gallium/active nitrogen flux ratio of 1.4. The AlN layers were grown with an aluminum/active nitrogen flux ratio ≈1.

The device fabrication began with a Ti/Al/Ni/Au (30 nm/200 nm/40 nm/20 nm) ohmic-first process that used a premetallization etch [15] to recess the contact metal prior to annealing at 800 °C. After annealing, the ohmic contact resistance was measured to be 0.3–0.4 Ω-mm using circular transfer length method patterns. Following standard Cl_2/BCl_3-based dry etch mesa isolation, a 7-nm HfO_2 gate insulator was blanket deposited using tetrakis (ethylmethyl) amino hafnium (TEMAHf) and water at 250 °C by atomic layer deposition. Submicrometer Ni/Au (20 nm/300 nm) T-shaped gates were defined by electron-beam lithography. The device L_{SD} was 3 μm, gate width W_G was 2×75 μm, and L_G were 0.1, 0.14, and 2 μm. For the submicrometer T-gates, the gate head length was 0.5 μm. All dimensions were measured by scanning electron microscopy.

III. Results and Discussion

Room-temperature on-wafer Hall effect measurements were taken before and after HfO_2 deposition to determine low-field transport properties. Prior to oxide deposition, the average sheet resistance R_{sh} was 194 Ω/sq with a 2DEG density of $n_s = 1.9 \times 10^{13}$ cm^{-2} and mobility of 1700 cm^2/V · s. Following oxide deposition, R_{sh} dropped to 164 Ω/sq with an associated increase in $n_s = 2.4 \times 10^{13}$ cm^{-2} and a slight reduction in mobility to 1600 cm^2/V · s. With the 2DEG n_s well in excess of 10^{13} cm^{-2} in the access regions, we suspect that there is sufficient Debye screening of charged dislocations and that the resulting mobility is therefore limited by polar optical phonon scattering and interfacial roughness [1].

DC electrical characteristics for an $L_G = 100$ nm device are shown in Fig. 2. An OFF-state breakdown voltage of 35 V was measured with $V_{GS} = -7$ V and 1 mA/mm of drain leakage current. Fig. 2(b) shows the transfer characteristics for the 100-nm device with a maximum current density of 1.5 A/mm, a threshold voltage of approximately −6.3 V, and a subthreshold swing of 162 mV/dec (not shown). Minimal hysteresis (< 100 mV) was observed when the transfer curve was immediately swept in the reverse direction after an initial trace. The peak transconductance $g_{m,max}$ was measured to be 347 mS/mm. Intrinsic $g_{m,max}$ was estimated to be 419 mS/mm when the voltage drops across R_s were accounted for. The sharp asymmetric shape of the transconductance curve is not fully understood at this time but is likely related to the dynamic access resistance [16] or the carrier energy clamping due to optical phonon emission [17].

Small-signal characteristics for a MOS-HEMT with $L_G = 100$ nm, with pad parasitics deembedded, are shown in Fig. 3(a). $f_T = 165$ GHz and $f_{max} = 171$ GHz were determined by −20-dB/dec extrapolation of the small-signal current gain, $|h_{21}|$, and the maximum available gain (MAG), respectively. Prior to deembedding of probe pad parasitics (determined by cold field-effect transistor method [18]), the extrinsic f_T/f_{max} were 120 GHz/170 GHz for the $L_G = 100$ nm device in Fig. 3(a). Pad deembedded f_T/f_{max} values of 112 GHz/134 GHz and 10 GHz/27 GHz were extracted for the 140 nm and 2-μm-L_G devices, respectively. Fig. 3(b) compares the small-signal f_T results from this study to literature values for AlN/GaN HEMTs. Despite having a relatively long $L_{SD} = 3$ μm, we observe that the f_T values from the devices in this study are in line with the highest reported values at coincident L_G. To investigate whether the improved small-signal performance of our devices was due to reduced parasitic effects or shorter intrinsic delay, small-signal modeling of the measured S-parameter data was conducted.

Fig. 4 summarizes results of small-signal equivalent circuit model fitting to the measured S-parameters of the $L_G = 100$ nm MOS-HEMT in Fig. 3(a). [19]. Of the delays, the parasitic charging [defined as $C_{gd} \cdot (R_s + R_d)$] and the channel charging [calculated as $(g_{ds}/g_m) \cdot (C_{gd} + C_{gs}) \cdot (R_s + R_d)$]

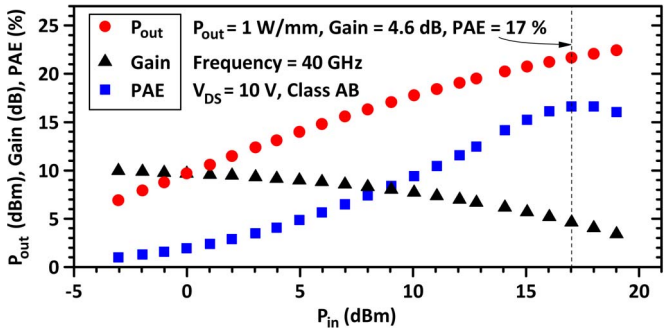


Fig. 5. The 40-GHz power sweep of an $L_G = 140$ nm AlN/GaN device.

are relatively small percentages of the total delay (∼11% and 4%, respectively). The drain delay, i.e., C_{gd}/g_m, is more substantial (19%) and potentially arises from the large drain bias (8 V) causing an expansion of the drain-side depletion region. The largest contributor to the total delay, according to our modeling, is the intrinsic gate transit time, i.e., C_{gs}/g_m. By dividing L_G by the intrinsic gate transit time, intrinsic v_e is calculated to be 1.53×10^7 cm/s for the 100-nm device. An identical analysis of a 140-nm device found the intrinsic v_e to be 1.49×10^7 cm/s, with intrinsic gate transit and total delay times of 0.94 and 1.36 ps, respectively. These values of v_e are among the highest reported for AlN/GaN HEMTs, which range from $0.8-1.5 \times 10^7$ cm/s [2], [4], [12]. In the case of the highest reported v_e [4], velocity enhancement was achieved by laterally scaling the device to increase the lateral electric field across the intrinsic device. We speculate that the elevated velocity in this study is *not* due to velocity enhancement but, instead, is a result of using epitaxial material grown on HVPE GaN, where low dislocation densities in the low-field portion of the intrinsic device result in minimal mobility degradation when the gate is biased for peak f_T (and $n_{\rm sh}$ is reduced $< 1 \times 10^{13}$ cm^{-2}) [20]. In higher dislocation density material, the depletion of the 2DEG underneath the gate metal, when biased for peak f_T, could significantly reduce the Debye screening of charged dislocations and render electron transport susceptible to Coulombic scattering and, consequently, lower intrinsic v_e.

To evaluate the large-signal potential of these devices, 500-ns pulsed gate lag measurements were performed at quiescent biases of $V_{DS} = 10$ V and $V_{GS} = -7$ V and showed gate lag ratios (pulsed $I_{\rm DSS}$/dc $I_{\rm DSS}$) of 0.8–1.0 for all devices in this study. Subsequent on-wafer 40-GHz load-pull measurements taken on a 140-nm device biased in class AB ($V_{DS} = 10$ V, and $V_{GS} = -4.5$ V) gave the results shown in Fig. 5. At the peak power-added efficiency (PAE) of 17%, the gain was 4.6 dB, and the output power density was 1 W/mm. This result shows the potential for AlN/GaN HEMTs to produce millimeter-wavelength power.

IV. Conclusion

To the best of our knowledge, this is the first demonstration of an AlN/GaN MOS-HEMT on freestanding GaN. Epitaxial growth on HVPE GaN has been shown to yield submicrometer devices with excellent dc and RF performance. Reflective of the material quality, a high value of intrinsic average electron velocity ($v_e = 1.5 \times 10^7$ cm/s) was extracted for these devices.

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