AlN/GaN insulated gate HEMTs with HfO_2 gate dielectric

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AlN/GaN single heterojunction MOS-HEMTs grown by molecular beam epitaxy have been fabricated utilising HfO_2 high-K dielectrics deposited by atomic layer deposition. Typical DC transfer characteristics of 1.3 μm gate length devices show a maximum drain current of 950 mA/mm and a transconductance of 210 mS/mm with gate currents of 5 μA/mm in pinch-off. Unity gain cutoff frequencies, f_t and f_{max}, were measured to be 9 and 32 GHz, respectively.

Introduction: The AlN/GaN high electron mobility transistor (HEMT) is an attractive structure for extending the frequency performance of III-N based transistors. This stems from the very thin AlN barrier layer that is utilised, which permits a significant reduction in gate length while maintaining an appropriate gate-to-channel aspect ratio to mitigate short channel effects. Recently, the AlN/GaN HEMT has shown its potential by demonstrating some of the highest current densities and transconductances in a single heterostructure with appreciable cutoff frequencies [1–3]. However, a major issue in such structures is high Schottky gate currents due to tunnelling through the thin AlN cap, which necessitates the insertion of a gate insulator. High-K dielectrics have matured to where they are now of interest in application to MOS-gated devices [4]. In this Letter, the first demonstration of an ALD deposited HfO_2 gate-dielectric AlN/GaN MOS-HEMT is presented. Owing to the insertion of a 3.6 nm HfO_2 layer, the gate current in these devices was extremely low, typically 5 μA/mm. This is particularly noteworthy since this result was achieved in a structure with a thin 4.5 nm AlN barrier layer. In this Letter, we report on DC, RF and power performance of the AlN/GaN HEMT.

Device growth and fabrication: The AlN/GaN heterojunctions were grown by plasma assisted MBE on 2 inch diameter semi-insulating 4H-SiC substrates. The procedures for SiC substrate preparation are similar to those we have described elsewhere [5, 6]. The 60 nm-thick AlN nucleation layer was grown, followed by subsequent unintentionally doped (UID) GaN buffer and AlN barrier layers with thicknesses of 1 μm and 4.5 nm, respectively. The AlN barrier thickness was chosen on the basis of work by Cao *et al.* who showed a minimum sheet resistance in single heterojunction AlN/GaN HEMTs with AlN thicknesses between 3–5 nm [7]. The GaN growth rate was determined to be 1.2 Å/s from optical reflectance measurements. All epitaxial layers were grown without interruptions.

Contactless resistance measurements on the unprocessed sample showed sheet resistances in the range 600–800 Ω/□, which we speculate is due to an AlN cap layer thickness variation across the wafer surface. Device fabrication was initiated by e-beam evaporation of Ti/Al/Ni/Au contact metallisation, which were annealed at 800°C for 30 s to form ohmic contacts. Contact resistances were found to be in the range 0.8–1.1 Ω mm, determined by circular transfer length method measurements. Mesa isolation was achieved via a BCl_3/Cl_2 plasma etch.

HfO_2 films were deposited from tetrakis (ethylmethyl) amino hafnium (TEM AHf) and water at 250°C using a hot wall stainless steel flow tube atomic layer deposition (ALD) reactor. The fixed volume approach as described elsewhere was used for the delivery of both reagents [8, 9]. The Ni/Au gate metallisation was then defined and deposited through standard photolithography and e-beam evaporation. A BCl_3/Cl_2 plasma etch was applied to open windows in the HfO_2 to access the ohmic metal for the final overlay metallisation. This was followed by the deposition of a 100 nm-thick PECVD SiN film and a subsequent photolithographic patterning and SF_6 plasma etch to open windows to the overlay metal contacts for probing.

Device characterisation: Hall effect measurements were performed both prior to HfO_2 deposition and after gate metallisation. R_{sh} decreased on average by 12% through an increase in sheet density, suggesting the partial passivation of surface states. Room temperature 2DEG density and mobility after HfO_2 deposition was found to be 1.48×10^{13} cm^{-2} and 620 cm^2/Vs, respectively. No change in mobility was observed, which indicates the ALD HfO_2 is a low damage process. Fig. 1 shows two-terminal diode current density for both Ni/Au-AlN and Ni/Au-HfO_2 Schottky diodes with 150, 100 and 50 μm diameter diode dot sizes. A 7 to 8 order of magnitude reduction in diode current down to approximately 1 μA/cm2 was observed in the sample with the 3.6 nm HfO_2 dielectric compared to the sample without the dielectric layer, indicating excellent gate-current suppression due to the dense ALD dielectric. It should be noted that, owing to high reverse bias Schottky diode current for the uninsulated Ni/Au-AlN diodes, output characteristics of HEMTs with such gates could not be taken and therefore are not compared. This is consistent with other reports in literature [1–3].

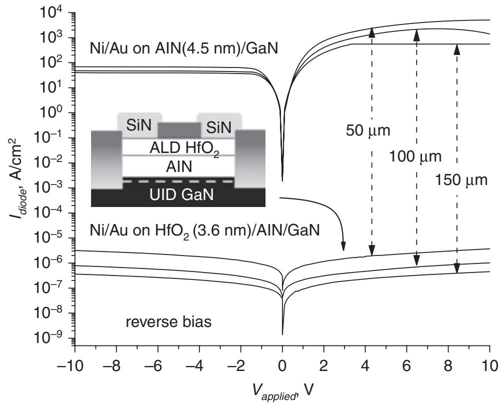

Fig. 1 *Current density comparison of Ni/Au Schottky on AlN/GaN (above) and HfO_2/AlN/GaN (below) diodes*

Each curve set demonstrates typical values for 150, 100 and 50 μm diameter dots
Inset: Insulated gate structure

Representative drain characteristics for 1.3 μm gate length (L_G), 150 μm gate width (W_G), and 5 μm source–drain spacing MOS-HEMT are shown in Fig. 2. As seen in the Figure, a current density of ~800 mA/mm at $V_{GS} = 0$ V was measured. A maximum drain–source current of 950 mA/mm at $V_{GS} = +4$ V and transconductance of 210 mS/mm at $V_{DS} = +10$ V was measured despite the high sheet and contact resistances (not shown). Analysis of capacitance–voltage characteristics of the HfO_2/AlN stacked capacitor confirmed the dielectric constant of the HfO_2 to be ~20, which is typical of ALD HfO_2. As shown in Fig. 2*a*, the MOS-HEMTs have excellent pinch-off characteristics, demonstrating that leakage current through the AlN barrier is dramatically suppressed by the ALD HfO_2 gate insulator. The threshold voltage is −4.1 V. In deep pinch-off ($V_{GS} = -7$ V, $V_{DS} = 10$ V, $I_{DS} = 7$ μA/mm) the gate leakage current was measured to be 5 μA/mm (not shown). The off-state breakdown voltage was >25 V with the criterion of $I_{DS} = 1$ mA/mm under pinch-off conditions. S-parameter measurements at a quiescent bias of $V_{DS} = 15$ V and $V_{GS} = -1.5$ V yield a current gain cutoff frequency, f_t, of 9 GHz and a power gain cutoff frequency, f_{max}, of 32 GHz, as shown in Fig. 2*b*. A Focus Microwaves load-pull system was used to measure the output power at 2 GHz. An output power of 2.6 W/mm and a PAE of 33% was measured.

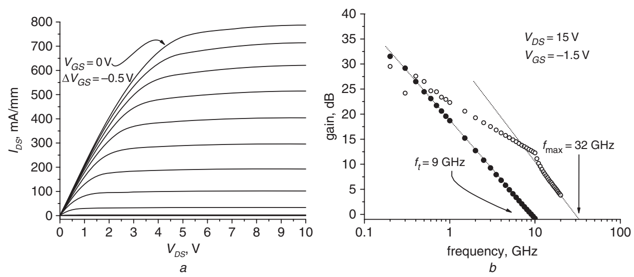

Fig. 2 *IV drain characteristics*

a $L_g = 1.3$ μm, $W_g = 150$ μm. Threshold voltage occurs at $V_{GS} = -4.1$ V
b Small-signal measurements

Conclusions: An AlN/GaN MOS-HEMT employing a 3.6 nm ALD HfO_2 gate dielectric has been demonstrated. Despite higher sheet and contact resistances, 1.3 μm gate lengths and a non-optimised growth, these devices showed maximum drain currents of 950 mA/mm and

210 mS/mm transconductance. Unity gain cutoff frequencies, f_t and f_{max} were measured to be 9 and 32 GHz for 1.3 μm long gates, respectively. Most notable was the reduction in gate current to 5 μA/mm in deep pinch off conditions ($V_{GS} = -7$ V, $V_{DS} = 10$ V) in a structure with an overall barrier thickness of 8 nm. Such performance exemplifies the potential for ultrathin AlN/GaN heterostructures in conjunction with ALD HfO_2 dielectric layers for the application to high-speed, high-power III-N technology.

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